MODEL NAME : GDC31/GDC41/GDC50

PCB NO : LA-K371P

BOM P/N : 431ANU31LXX

X12 TGL UMA MB

Tiger Lake U42 UP3

2020-10-28

REV : 1.0 (A00)

@ : Nopop Component
EMI@ : EMI Component
@EMI@ : EMI Nopop Component
ESD@ : ESDComponent
@ESD@ : ESD Nopop Component
RF@ : RF Component
@RF@ : RF Nopop Component
CONN@ : Connector Component
MIPI60@ :MIPI Component
NMIPI60@ :Non MIPI Pop Component
VPRO@ : vPro Component
NVPRO@ : Non-vPro Component
WWAN@ : WWAN Component
@WWAN@ : WWAN Nopop Component
JUMP@ : Jump solder and short
@JUMP@ : Jump no solder
CPU@ : CPU
5107@ : MEC5200 Component
5200@ : MEC5200 Component
750@ : NUVOTON NPCT750 TPM Component
ST33@ : ST ST33HTPH TPM Component

5107ES@ : MEC5107 ES Component
5107NES@ : MEC5107 Non-ES Component

Power CKT : MONTREUX_MB_TGL_PWR_20201013A
GPIO map : X12_TGL_U GPIO map Rev1.0_20200910

DELL CONFIDENTIAL/PROPRIETARY

MB PCB

Part Number	Description
DA8001N200S	PCB 30K DB-2755P REV0 D/B S

Layout Dell logo

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REV:X00
PWB:

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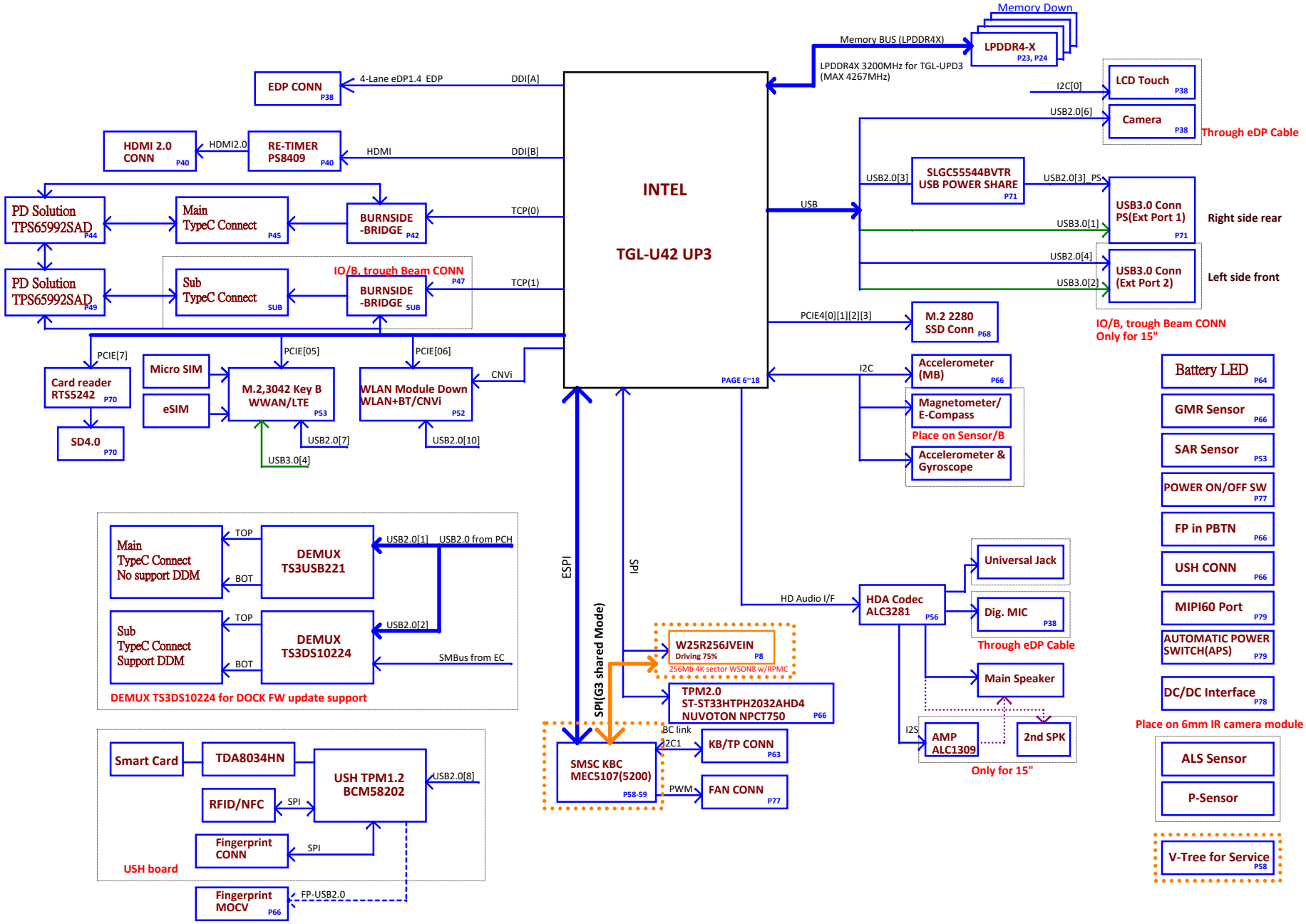
Compal Electronics, Inc.

Title: Cover Sheet

Size | Document Number: LA-K371P | Rev: 1.0

Date: Wednesday, October 28, 2020 | Sheet 1 of 125

X12 7000 TGL Block Diagram



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Title	Block Diagram
Size	Document Number: LA-K371P
Rev	1.0
Date:	Wednesday, October 28, 2020
Sheet	2 of 125

POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	PRIM PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S0ix/Moff	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF
S0ix (Suspend to RAM) / M-OFF	HIGH	HIGH	HIGH	LOW	ON	ON	ON	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB3.0	Gbe	PCIE	SATA	DESTINATION
USB3.0-1		PCIE-1		JUSB1
USB3.0-2		PCIE-2		JUSB2
USB3.0-3		PCIE-3		NA
USB3.0-4		PCIE-4		M.2 3042(WWAN)
		PCIE-5		M.2 3042(LTE)
	V	PCIE-6		WLAN
	V	PCIE-7		CARD READER
	V	PCIE-8		NA
		PCIE-9		NA
		PCIE-10		NA
		PCIE-11	SATA-0	NA
		PCIE-12	SATA-1	NA
PCIE4-1~4				M.2 2280 SSD

USB PORT#	DESTINATION
1	Type-C Port 1
2	Type-C Port 2
3	JUSB1(RIGHT)
4	JUSB2(LEFT)
5	NA
6	Camera
7	M.2 3042(WWAN)
8	USH
9	NA
10	M.2 2230(BT)

PM TABLE

State \ power plane	+3.3V_RTC_LDO +5V_ALW +5V_ALW2 +3.3V_ALW +3.3V_ALW2 +3.3V_PRIM +1.8V_PRIM +3.3V_ALW_DSW +VCC_VNNEXT_1P05 +VCC_V1P05EXT_1P05	+1.1V_MEM +1.8V_MEM +1.05V_VCCST	+1.05V_VCCSTG* +3.3V_RUN +5V_RUN +1.8V_RUN +1.2V_RUN +0.6V_DDR_VTT	+RTC_CELL
S0	ON	ON	ON	ON
S0ix	ON	ON	OFF	ON
S5 S4/AC	ON	OFF	OFF	ON
S5 S4/DC only	OFF	OFF	OFF	ON

*VCCSTG can be turned off when the processor is in C10

Figure 2. Flexible HSIO Lane Multiplexing in PCH-LP (UP3)

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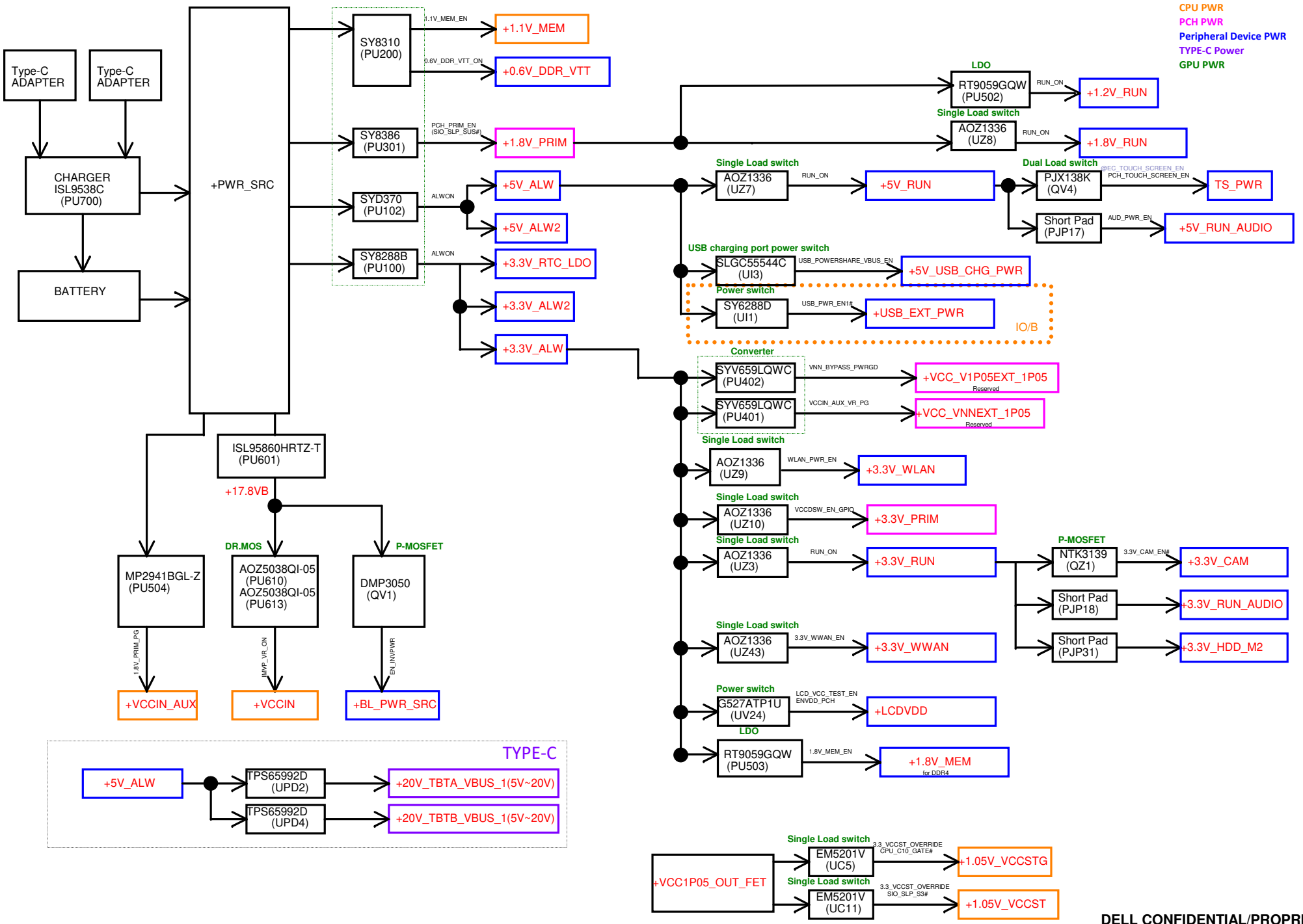
Compal Electronics, Inc.

Title: Port assignment

Size | Document Number: LA-K371P | Rev: 1.0

Date: Wednesday, October 28, 2020 | Sheet 3 of 125



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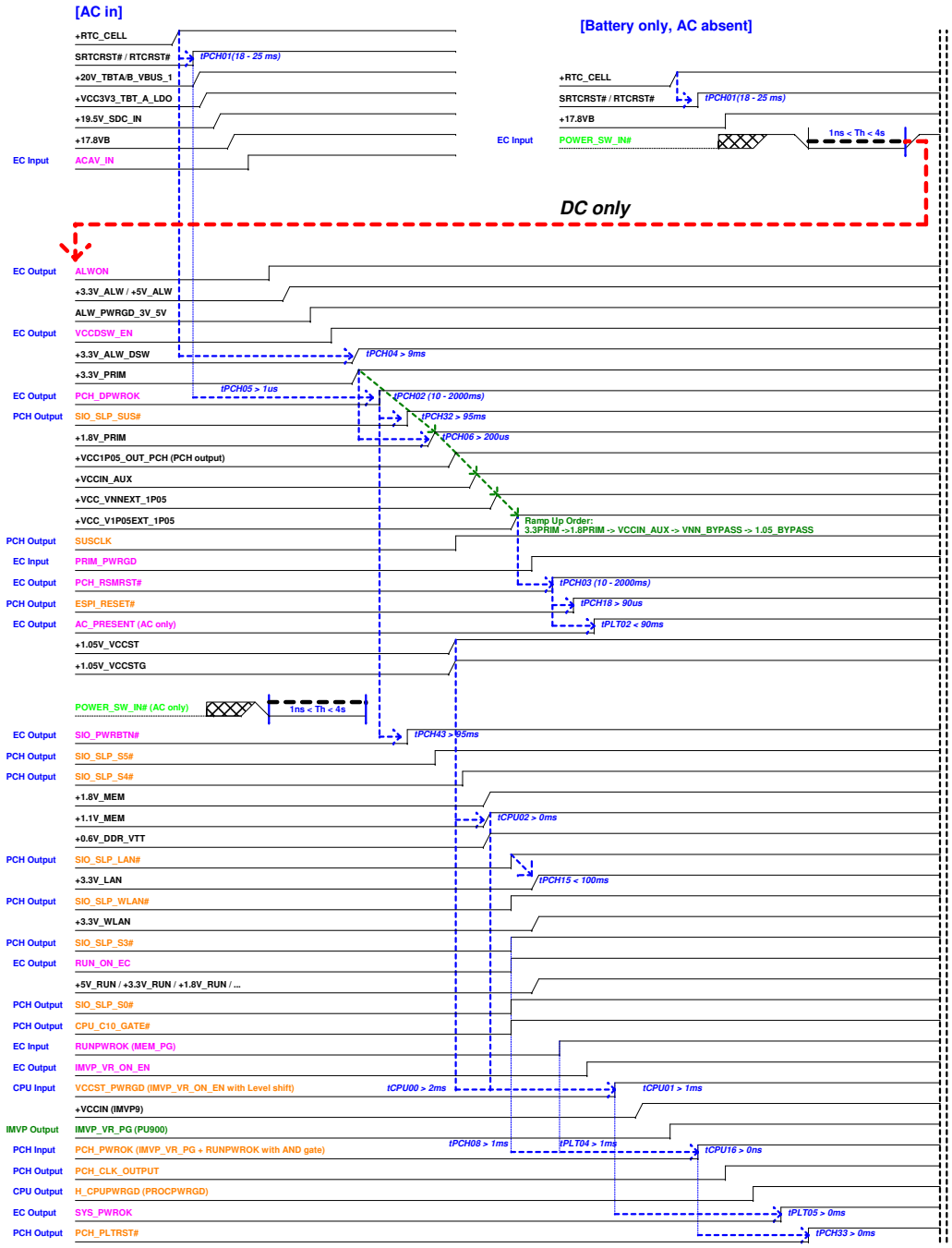
Compal Electronics, Inc.

Title: Power rails

Size | Document Number: LA-K371P | Rev: 1.0

Date: Wednesday, October 28, 2020 | Sheet 4 of 125

Power Sequence
G3 -> S0 Non deep



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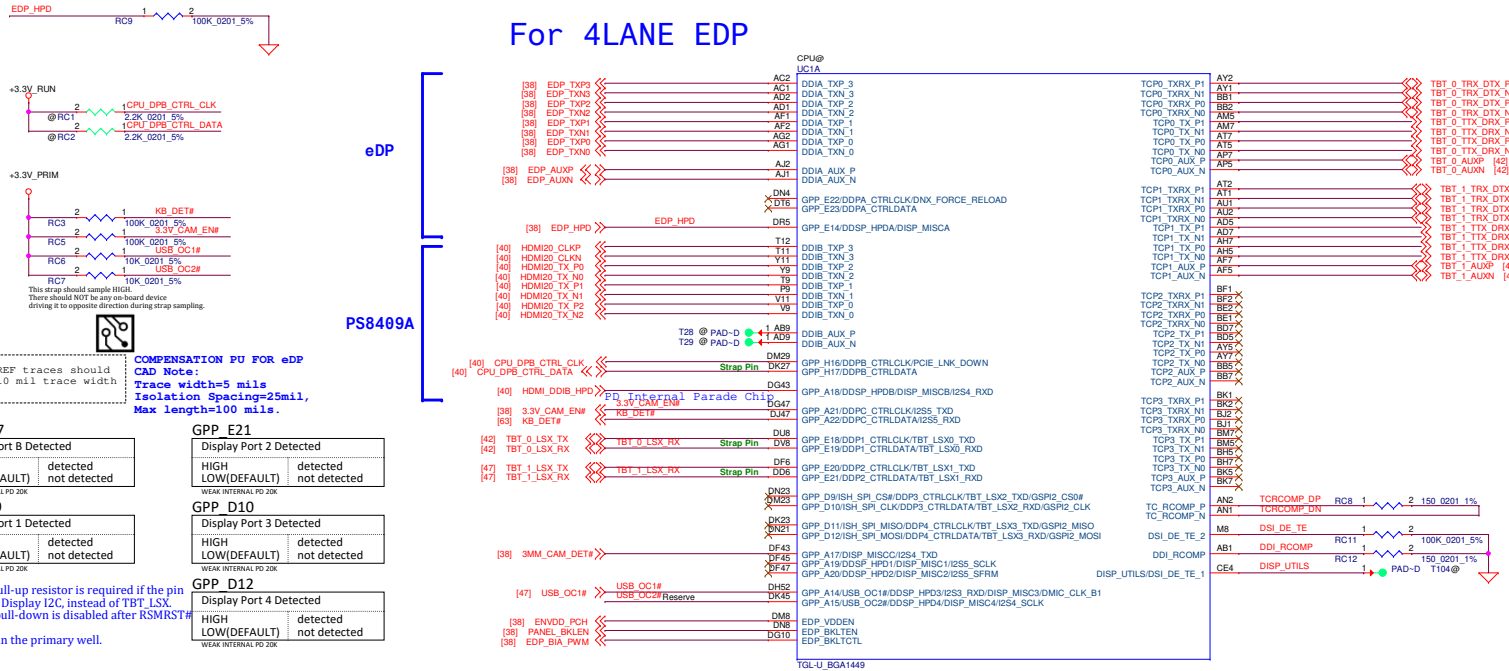
Compal Electronics, Inc.

Title: Power Sequence

Size | Document Number: LA-K371P | Rev: 1.0

Date: Wednesday, October 28, 2020 | Sheet 5 of 125

For 4LANE EDP



GPP_H17

Display Port B Detected	
HIGH	detected
LOW(DEFAULT)	not detected

WEAK INTERNAL PD 20K

GPP_E21

Display Port 2 Detected	
HIGH	detected
LOW(DEFAULT)	not detected

WEAK INTERNAL PD 20K

GPP_E19

Display Port 1 Detected	
HIGH	detected
LOW(DEFAULT)	not detected

WEAK INTERNAL PD 20K

GPP_D10

Display Port 3 Detected	
HIGH	detected
LOW(DEFAULT)	not detected

WEAK INTERNAL PD 20K

GPP_D12

Display Port 4 Detected	
HIGH	detected
LOW(DEFAULT)	not detected

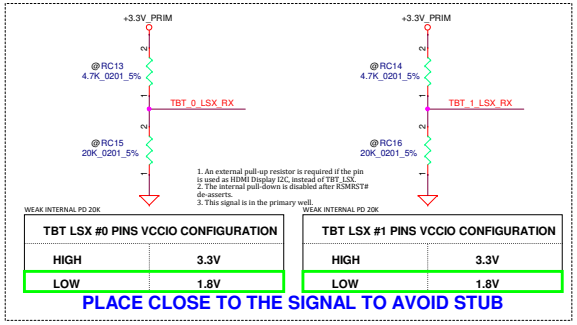
WEAK INTERNAL PD 20K

1. An external pull-up resistor is required if the pin is used as HDMI Display I2C, instead of TBT_LSX.
2. The internal pull-down is disabled after RSMRST# de-asserts.
3. This signal is in the primary well.

Table 35. DDI Ports Availability

SKU	UP4 Processor Line Quad Core GT2	UP3 Processor Line Quad Core GT2
DDI A	eDP*/MIPI_0	eDP*/MIPI_0
DDI B	DP*/HDMI*/MIPI_1	DP*/HDMI*
TCP0	DP*/HDMI*	DP*/HDMI*
TCP1	DP*/HDMI*	DP*/HDMI*
TCP2	DP*/HDMI*	DP*/HDMI*
TCP3	N/A	DP*/HDMI*

Note: HBR3 supported on TCP ports only.



TBT LSX #0 PINS VCCIO CONFIGURATION	
HIGH	3.3V
LOW	1.8V

TBT LSX #1 PINS VCCIO CONFIGURATION	
HIGH	3.3V
LOW	1.8V

PLACE CLOSE TO THE SIGNAL TO AVOID STUB

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Compal Electronics, Inc.

Title: MCP(1/13)TCSS,EDP,DDI

Size: Document Number: LA-K371P Rev: 1.0

Date: Wednesday, October 28, 2020 Sheet 6 of 125

BOOT STRAP (0000) : enable eSPI

BOOT STRAP 3

GPP_H2 (Weak internal PD 20K)

This is bit 3 of a total of 4-bit encoded pin straps for boot configuration.

BOOT STRAP 2

GPP_H1 (Weak internal PD 20K)

This is bit 2 of a total of 4-bit encoded pin straps for boot configuration.

BOOT STRAP 1

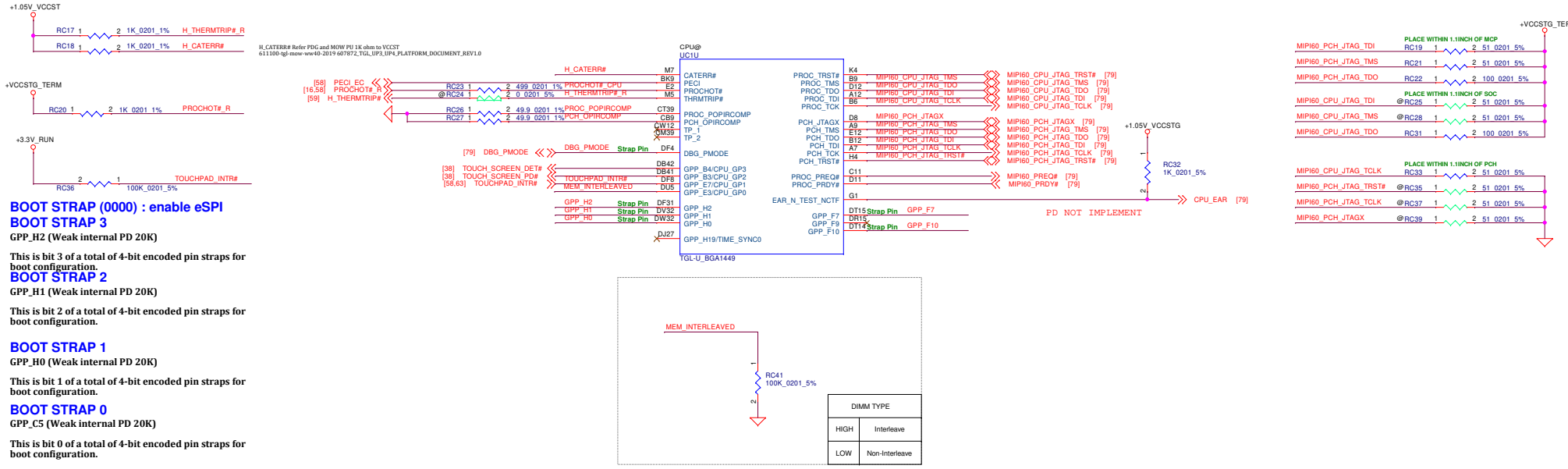
GPP_H0 (Weak internal PD 20K)

This is bit 1 of a total of 4-bit encoded pin straps for boot configuration.

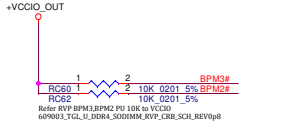
BOOT STRAP 0

GPP_C5 (Weak internal PD 20K)

This is bit 0 of a total of 4-bit encoded pin straps for boot configuration.

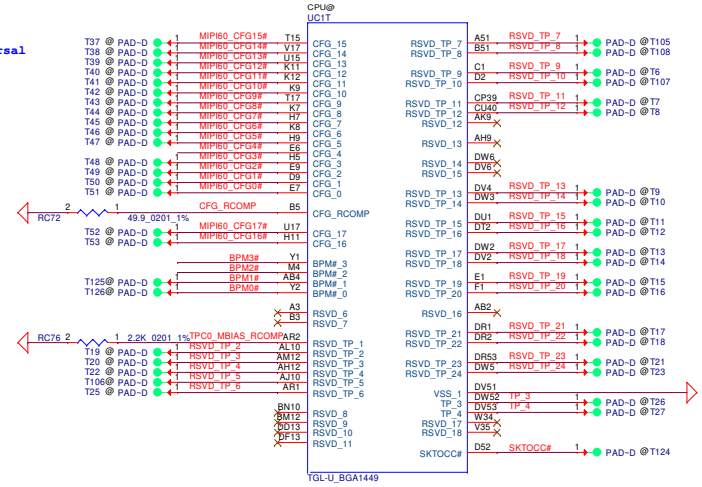


BOOT STRAP 3	BOOT STRAP 2	BOOT STRAP 1	Reserved	Reserved	Reserved
GPP_H2 (Weak internal PD 20K) **This is bit 3 of a total of 4-bit encoded pin straps for boot configuration.**	**GPP_H1 (Weak internal PD 20K)** **This is bit 2 of a total of 4-bit encoded pin straps for boot configuration.**	**GPP_H0 (Weak internal PD 20K)** **This is bit 1 of a total of 4-bit encoded pin straps for boot configuration.**	**GPP_F7 (Weak internal PD 20K)**	**GPP_F10 (Weak internal PD 20K)**	**DBG_PMODE (Internal 20 K Pull UP)** Follow PDG 1K PU to PCH VCC1p05_OUT_FET 607872_TGL_UP3_UP4_RN_Rev1p0
GPP_H2 @RC42 1 2 4.7K_0201_5% +3.3V_PRIM	GPP_H1 @RC43 1 2 4.7K_0201_5% +3.3V_PRIM	GPP_H0 @RC44 1 2 4.7K_0201_5% +3.3V_PRIM	GPP_F7 @RC45 1 2 4.7K_0201_5% +3.3V_PRIM	GPP_F10 @RC46 1 2 4.7K_0201_5% +3.3V_PRIM	DBG_PMODE RC47 1 2 1K_0201_5% +V1.05A_MIPI60



MIPI60_CFG4#
eDP enable Strap
0: ENABLED
1: DISABLED; (DEFAULT)

CFG[14] PCIe Gen4 Lane Reversal
1: Normal(Default)
0: Reversed



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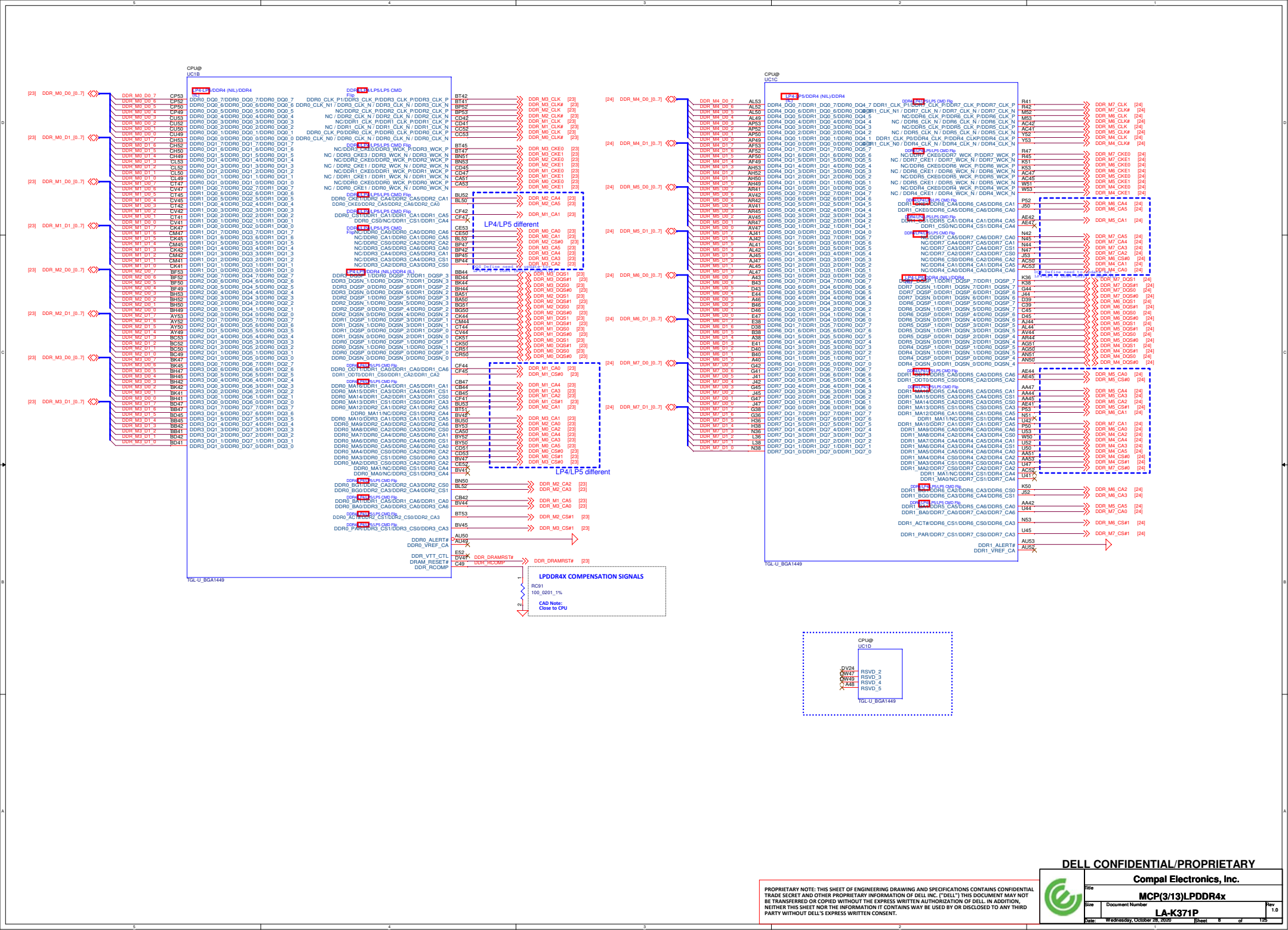
Compal Electronics, Inc.

Title: MCP(2/13)MISC,MIPI60

Size | Document Number: LA-K371P | Rev: 1.0

Date: Wednesday, October 28, 2020 | Sheet 7 of 125



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Compal Electronics, Inc.

Title: MCP(3/13)LPDDR4x

Size: Document Number: LA-K371P

Rev: 1.0

Date: Wednesday, October 28, 2020

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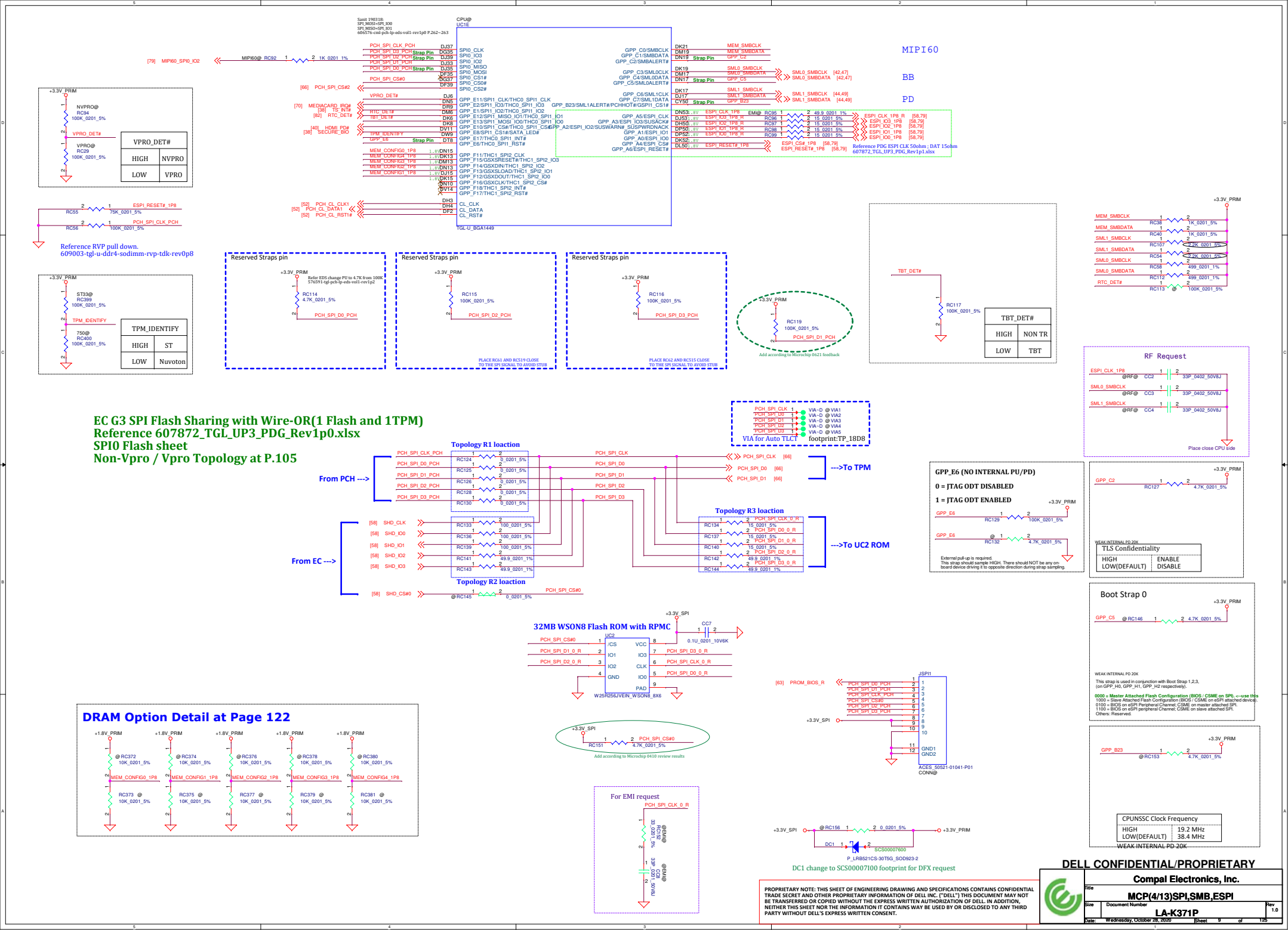


VPRO_DET#	
HIGH	NVPRO
LOW	VPRO

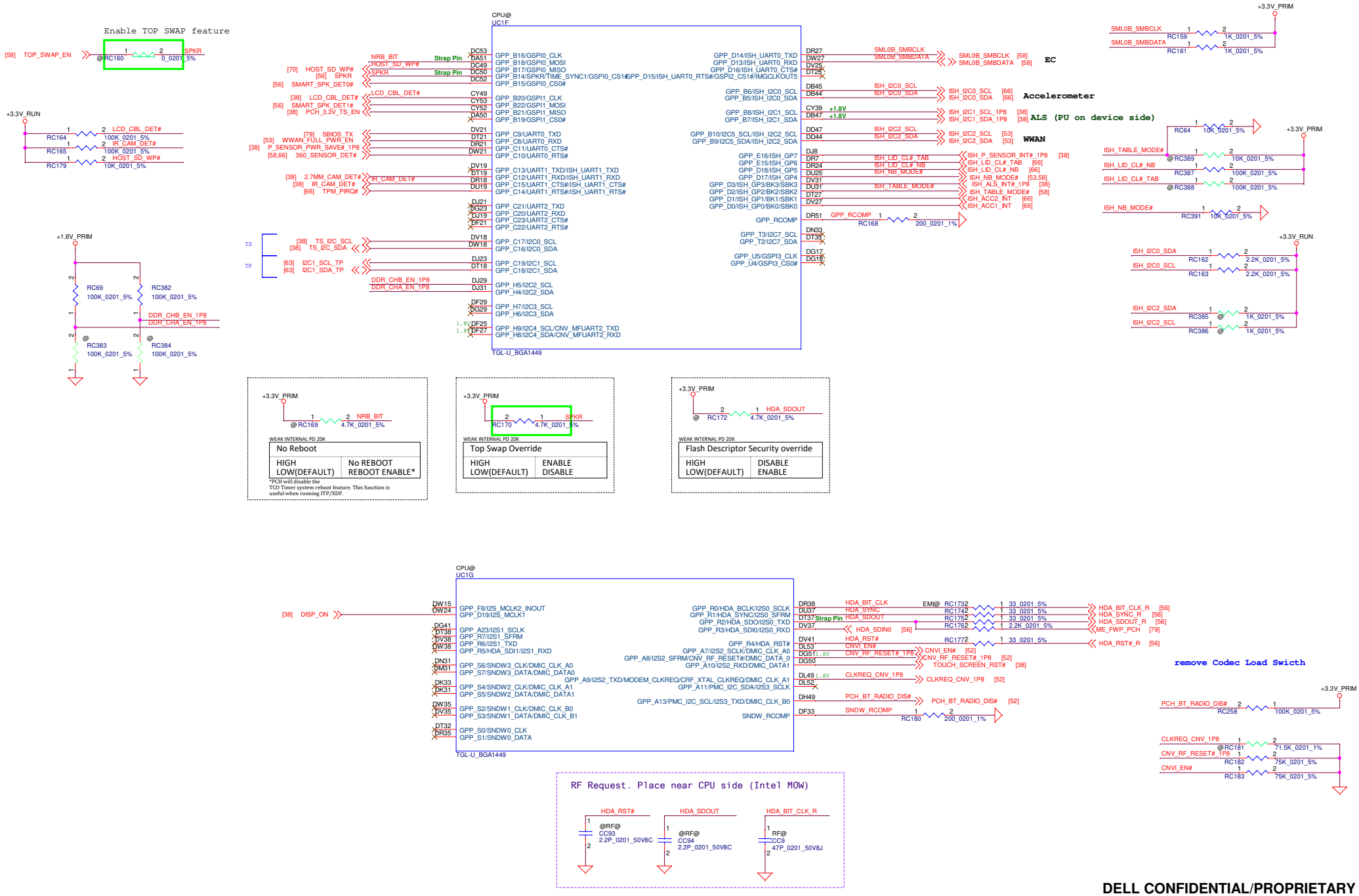
TPM_IDENTIFY	
HIGH	ST
LOW	Nuvoton

TBT_DET#	
HIGH	NON TR
LOW	TBT

TLS Confidentiality	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

CPUNSSC Clock Frequency	
HIGH	19.2 MHz
LOW(DEFAULT)	38.4 MHz

WEAK INTERNAL PD 20K



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Compal Electronics, Inc.

Title: MCP(5/13)HDA,I2C,ISH

Size | Document Number: LA-K371P | Rev: 1.0

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+3.3V_ALW_DSW Source

+3.3V_ALW_DSW — @RC270 1 — 2 0_0402_5% — +3.3V_PRIM

Card Reader --->
M.2 3042 WWAN--->
M.2 2230 WLAN--->
M.2 2280 SSD--->

[70] CLK_PCIE_P4 — BW4 — CLKOUT_PCIE_P4
[70] CLK_PCIE_N4 — BW5 — CLKOUT_PCIE_N4
CLKOUT_PCIE_P3 — CL7
CLKOUT_PCIE_N3 — CL8
[53] CLK_PCIE_P2 — CB4 — CLKOUT_PCIE_P2
[53] CLK_PCIE_N2 — CB5 — CLKOUT_PCIE_N2
[52] CLK_PCIE_P1 — BY4 — CLKOUT_PCIE_P1
[52] CLK_PCIE_N1 — BY3 — CLKOUT_PCIE_N1
[68] CLK_PCIE_P0 — CN7 — CLKOUT_PCIE_P0
[68] CLK_PCIE_N0 — CN8 — CLKOUT_PCIE_N0
XCLK_BIASREF — RC205 2 — 1 60.4_0201_1% — DJ5

CPU@ UC1K
CLKOUT_PCIE_P6 — BW1
CLKOUT_PCIE_N6 — BW2
CLKOUT_PCIE_P5 — CB2
CLKOUT_PCIE_N5 — CB1
GPP_F19/SRCCLKREQ6# — DU14 — CAM_MIC_CBL_DET#
GPP_H11/SRCCLKREQ5# — DF25 — CLKREQ_PCIE#5 — CAM_MIC_CBL_DET# [38]
GPP_H10/SRCCLKREQ4# — DG25 — CLKREQ_PCIE#4 — CLKREQ_PCIE#4 [70]
GPP_D8/SRCCLKREQ3# — DT24 — CLKREQ_PCIE#3
GPP_D7/SRCCLKREQ2# — DT30 — CLKREQ_PCIE#2 — CLKREQ_PCIE#2 [53]
GPP_D6/SRCCLKREQ1# — DV30 — CLKREQ_PCIE#1 — CLKREQ_PCIE#1 [52]
GPP_D5/SRCCLKREQ0# — DW30 — CLKREQ_PCIE#0 — CLKREQ_PCIE#0 [68]
XTAL_OUT — DM1 — XTAL_PCH_38P4M_OUT
XTAL_IN — DL1 — XTAL_PCH_38P4M_IN
GPD8/SUSCLK — DW41 — SUSCLK — SUSCLK [52,68]
RTCX2 — DT47 — PCH_RTCX2
RTCX1 — DR47 — PCH_RTCX1
RTCRST# — DN37 — PCH_RTCRST# — PCH_RTCRST# [58,79]
SRTCRST# — DK37 — SRTCRST#
TGL-U_BGA1449

+3.3V_PRIM — RC192 2 — 1 100K_0201_5% — CAM_MIC_CBL_DET#

+3.3V_RUN
CLKREQ_PCIE#0 — RC1852 — 20K_0201_5%
CLKREQ_PCIE#1 — RC1872 — 20K_0201_5%
CLKREQ_PCIE#2 — RC1882 — 20K_0201_5%
CLKREQ_PCIE#3 — RC1892 — 20K_0201_5%
CLKREQ_PCIE#4 — RC1902 — 20K_0201_5%
CLKREQ_PCIE#5 — RC1912 — 20K_0201_5%
0418 Follow Dorest intel recommend change CLKREQ pull up to 20K from 10K.
20200312 Follow Intel review RC187 change to 10k

@CC13 2 — 1 0.1U 16V K X5R 0201 — SUSCLK
RC203 1 — 2 20K_0201_5% — PCH_RTCRST# — RTC_CELL_PCH
CC15 1 — 2 1U_0201_6.3V6M
PCH_RTCRST# — RC206 1 — 2 20K_0201_5% — RTC_CELL_PCH
CC16 1 — 2 1U_0201_6.3V6M
@CMOS1 SHORT PADS-D

CMOS1 footprint change to SHORTPADS-NPM
CMOS1 must take care short & touch risk on layout placement

XTAL_PCH_38P4M_IN — EMI@ RC186 1 — 2 33_0201_5% — XTAL_38P4M_IN
CC10 1 — 2 10P_0201_50V8J
RC193 200K_0201_5% 1 — 2
Sanit 190318:Refer RVP is 200K ohm +-1% 609003_TGL_U_DDR4_SODIMM_RVP_CRB_SCH_REV0p8
YC1 38.4MHZ_10PF_8Y38420005 3 — 4 — 1 — 2
XTAL_PCH_38P4M_OUT — EMI@ RC194 1 — 2 33_0201_5% — XTAL_38P4M_OUT
CC11 1 — 2 10P_0201_50V8J
PCH_RTCX1 — RC199 1 — 2 0_0201_5% — PCH_RTCX1_R
CC13 1 — 2 8.2P_0201_25V8D
RC201 100K_0201_5% 1 — 2
Sanit 190318:Refer RVP is 10M ohm +-5% 609003_TGL_U_DDR4_SODIMM_RVP_CRB_SCH_REV0p8
YC2 32.768KHZ_9PF_X1A000141000200 ESR MAX=50k ohm 3 — 4 — 1 — 2
PCH_RTCX2 — RC202 1 — 2 0_0201_5% — PCH_RTCX2_R
CC14 1 — 2 8.2P_0201_25V8D
SUSCLK — @RC204 1 — 2 1K_0201_5%

RTC issue, update crystall part for integrate 8.2pF

+3.3V_ALW_DSW — RC207 2 — 1 10K_0201_5% — LAN_WAKE#

+3.3V_PRIM — RC214 2 — 1 1K_0201_5% — PCH_PCIE_WAKE#
PCH_PCIE_WAKE# Refer SCH check list pull up 1K to VCCDSW_3p3 607872_TGL_UP3_UP4_SchChk_Rev1p1

@RC217 2 — 1 10K_0201_5% — PCH_PWROK
Microchip suggest 100K PD
RC220 2 — 1 100K_0201_5% — PCH_DPWROK
@CC17 2 — 1 0.01U_0201_16V7
RC59 2 — 1 100K_0201_5% — PCH_RSMRST#_AND
RC57 2 — 1 100K_0201_5% — CPU_C10_GATE#

+3.3V_PRIM — CC92 1 — 2 0.1U_0201_10V6K
PCH_PLTRST# — 2 B — 1 A — 4 Y — PCH_PLTRST#_AND — PCH_PLTRST#_AND [38,42,52,53,68,70,79]
3 C — UC3 MC74VHC1G08EDFT2G_SC70-5
RC218 100K_0201_5% @ — 2

Need change PCH_PLTRST#_OB

SIO_SLP_SUS# — @RC370 1 — 2 0_0201_5% — PCH_PRIM_EN [90]

+3.3V_ALW_DSW — RC95 1K_0201_5% — SIO_PWRBTN# — CC96 0.1U_0201_10V6K

+3.3V_ALW_DSW
BATLOW# Refer SCH check list pull up 10K-100K VCCDSW_3p3 607872_TGL_UP3_UP4_SchChk_Rev1p0
PCH_BATLOW# — RC219 2 — 100K_0201_5%
AC_PRESENT — RC223 1 — 2 100K_0201_5%
AC_PRESENT is setting OD on EC side, so need pull up.
Refer SCH check list change to pull up 100K to DSW rail.
607872_TGL_UP3_UP4_SchChk_Rev1p1

Signals Required Cap or Pull-Down Resistor (607872_TGL_UP3_UP4_PLATFORM_DOCUMENT_REV1.0 P.172 P.173)

SIO_SLP_SUS# — RC225 — 0.33U_0201_6.3V6M — @CC18
SIO_SLP_S4# — RC227 — 0.33U_0201_6.3V6M — @CC19
SIO_SLP_S3# — RC229 — 0.33U_0201_6.3V6M — @CC21
SIO_SLP_A# — RC231 — 0.33U_0201_6.3V6M — @CC22
SIO_SLP_WLAN# — RC234 — 0.33U_0201_6.3V6M — @CC23
SIO_SLP_LAN# — RC236 — 0.33U_0201_6.3V6M — @CC24
SIO_SLP_S5# — @RC237
PCH_PLTRST# — RC238

Check!!
SIO_SLP_S0# RVP is PD 100K
SIO_SLP_S0# PDG is PU 100K

+3.3V_PRIM — RC366 — SIO_SLP_S0# — @RC249

CPU@ UC1L
SLP_SUS# — DV49 — SIO_SLP_SUS#
GPD10/SLP_S5# — DM43 — SIO_SLP_S5#
GPD5/SLP_S4# — DJ41 — SIO_SLP_S4# — [79]
GPD4/SLP_S3# — DJ43 — SIO_SLP_S3# — [25,79]
GPD6/SLP_A# — DR41 — SIO_SLP_A# — [16,59,79,92]
GPD9/SPI_WLAN# — DT44 — SIO_SLP_WLAN# — [79]
GPP_B12/SLP_S0# — DD42 — SIO_SLP_S0# — [78]
SLP_LAN# — DN39 — SIO_SLP_LAN# — [66,79]
RSMRST# — DM35 — PCH_RSMRST#_AND — [63]
SYS_RESET# — DD10 — SYS_RESET# — [79]
GPP_B13/PLTRST# — DD41 — PCH_PLTRST# — [66]
DSW_PWROK — DK35 — PCH_DPWROK — [63]
SYS_PWROK — DF10 — SYS_PWROK — [58]
PCH_PWROK — DN35 — PCH_PWROK — [97]
INTRUDER# — DM37 — INTRUDER# — [64]
SPIVCCIOSEL — DT49 — SPIVCCIOSEL — Strap Pin
PROCPWRGD — BM9 — H_CPUPWRGD
GPD3/PWRBTN# — DK41 — SIO_PWRBTN# — SIO_PWRBTN# [58]
GPD0/BATLOW# — DN41 — PCH_BATLOW#
GPD1/ACPRESENT — DK43 — AC_PRESENT — AC_PRESENT [58]
GPP_B11/PMCALERT# — CW40 — TBT_I2C_INT# — TBT_I2C_INT# [44,49]
GPP_H18/CPU_C10_GATE# — DN27 — CPU_C10_GATE# — CPU_C10_GATE# [16]
GPP_H3/SX_EXIT_HOLDOFF# — DG31 — SC_CAGE_DET# — SC_CAGE_DET# [66]
WAKE# — DK39 — PCH_PCIE_WAKE# — PCH_PCIE_WAKE# [58,59]
GPD2/LAN_WAKE# — DM41 — LAN_WAKE#
GPD11/LANPHYPC/DSWLDO_MON — DT41 — PinDT41 Lan_PHY_EN : MX no RJ45
GPD7 — DN43 — Strap Pin — PCH_TBT_PERST# — PCH_TBT_PERST# [42]
VCCSTPWRGOOD_TCSS — CE5 — VCCSTPWRGOOD_TCSS
VCCST_PWRGD — BP8 — VCCST_PWRGD_CPU
VCCST_OVERRIDE — BP9 — VCCST_OVERRIDE — RC232 2 — 1 60.4_0201_1% — VCCST_PWRGD [59]
GPP_F20/EXT_PWR_GATE# — DR12
GPP_F21/EXT_PWR_GATE2# — DW12
TGL-U_BGA1449

SC_CAGE_DET# — 2 — 1 — RC61 100K_0201_5% — +3.3V_RUN

+3.3V_PRIM — TBT_I2C_INT# — 1 — 2 — RC235 10K_0201_5%
MX remove option I2C to BB

+1.05V_VCCST — RC239 1K_0201_5%
VCCST_PWRGD 1.05V — @RC243 1 — 2 1K_0201_5% — PM_RSMRST_PWRGD_MIP60 [79]
PCH_RSMRST#_AND — MIP60@ RC244 1 — 2 1K_0201_5%
CPU Input, 1.05V — VCCSTPWRGOOD_TCSS — @RC245 1 — 2 0_0201_5% — VCCST_OVERRIDE_R [16]
PCH Output, 1.05V — VCCST_OVERRIDE — @RC248 1 — 2 0_0201_5%

Reserved Straps pin
+3.3V_ALW_DSW — @RC240 4.7K_0201_5% — PCH_TBT_PERST# — @RC368 20K_0201_5%
WEAK INTERNAL PD 20K
This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SPIVCCIOSEL — RC246 4.7K_0201_5%
There is no internal pull-up or pull-down on the strap. An external resistor is required.

SPI Operation Voltage Select	
HIGH	SPI voltage is 1.8V
LOW	SPI voltage is 3.3V

H_CPUPWRGD — ESD@ 10pF_0201_50V8J CC95
VCCST_PWRGD — ESD@ 10pF_0201_50V8J CC95
ESD Request:place near CPU side

PCH_PLTRST#_AND — ESD@ 0.47U_0402_16V7K CC27
For ESD solution

SYS_RESET# — @ESD@ 0.1U_0201_10V6K CC28
ESD Request:place near CPU side

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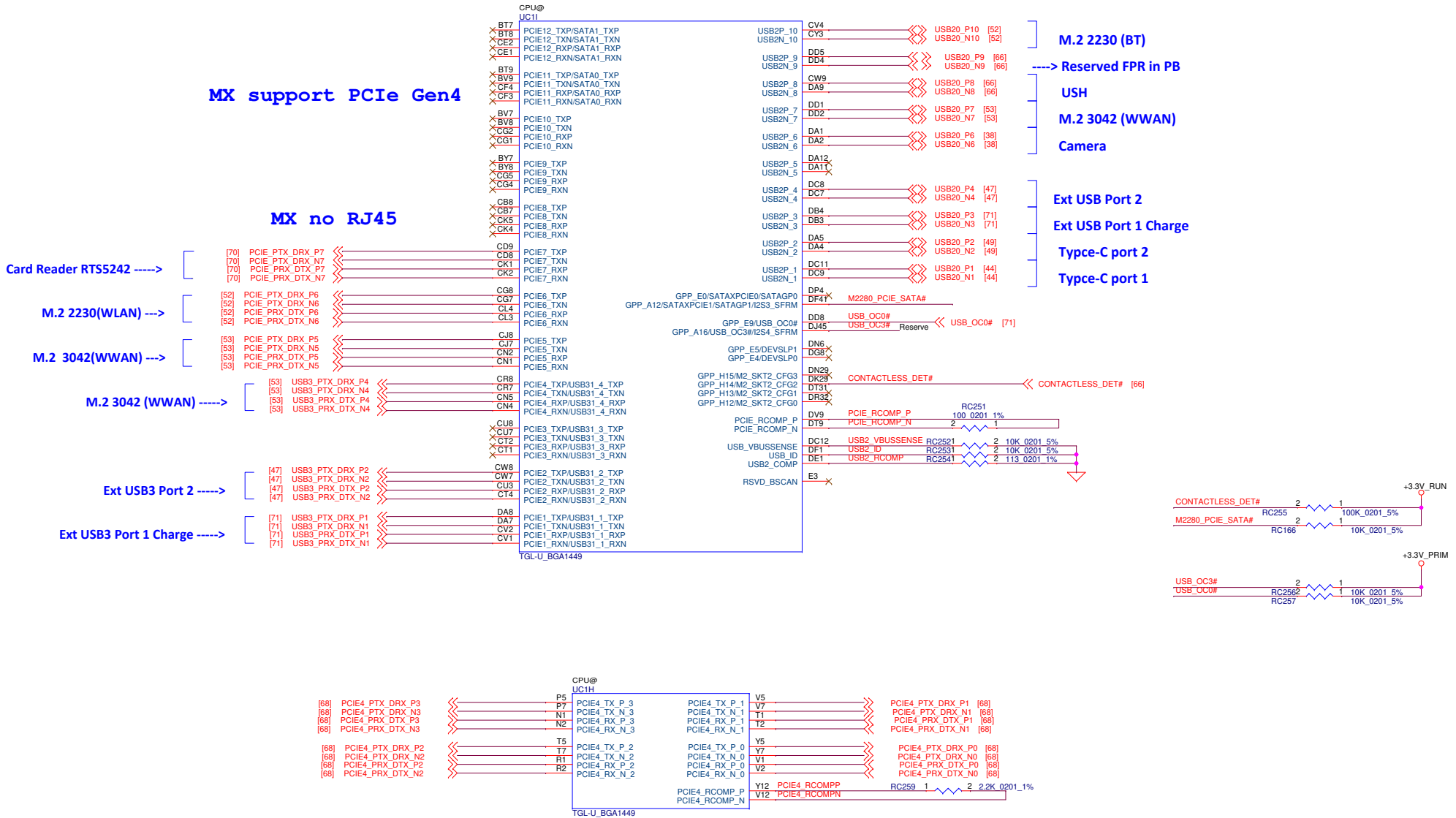
Compal Electronics, Inc.
Title: MCP(6/13)CLK,PM,RTC
Size: Document Number: LA-K371P
Rev: 1.0
Date: Wednesday, October 28, 2020
Sheet 11 of 125

TGL CSLP UMA(follow Compal_TGL_PortMap_20190829)



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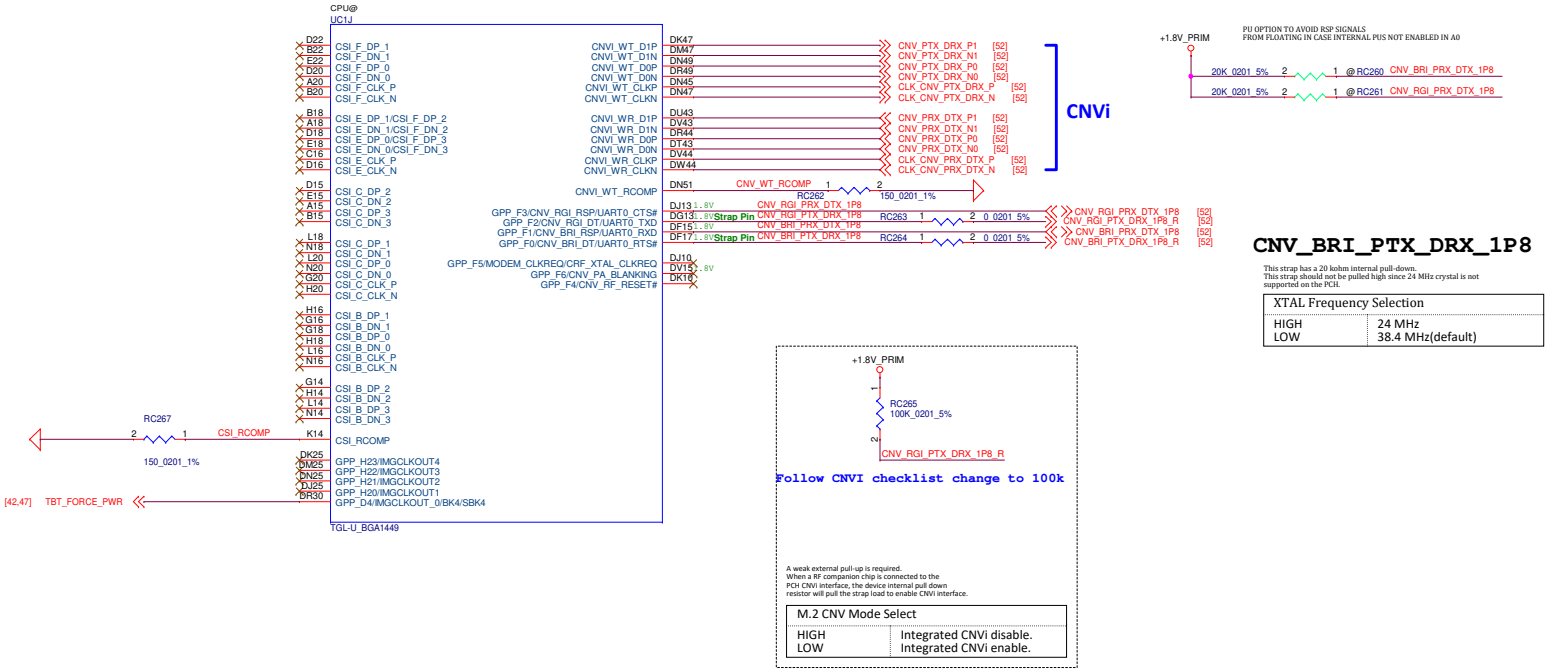
Compal Electronics, Inc.

Title: MCP(7/13)PCIE,USB,SATA

Size | Document Number: LA-K371P | Rev: 1.0

Date: Wednesday, October 28, 2020 | Sheet 12 of 125

CNVi reference 575882-intel-quasar-cnvio-schematic-checklist-rev3-1



CNV_BRI_PTX_DRX_1P8

This strap has a 20 kohm internal pull-down.
This strap should not be pulled high since 24 MHz crystal is not supported on the PCH.

XTAL Frequency Selection	
HIGH	24 MHz
LOW	38.4 MHz(default)

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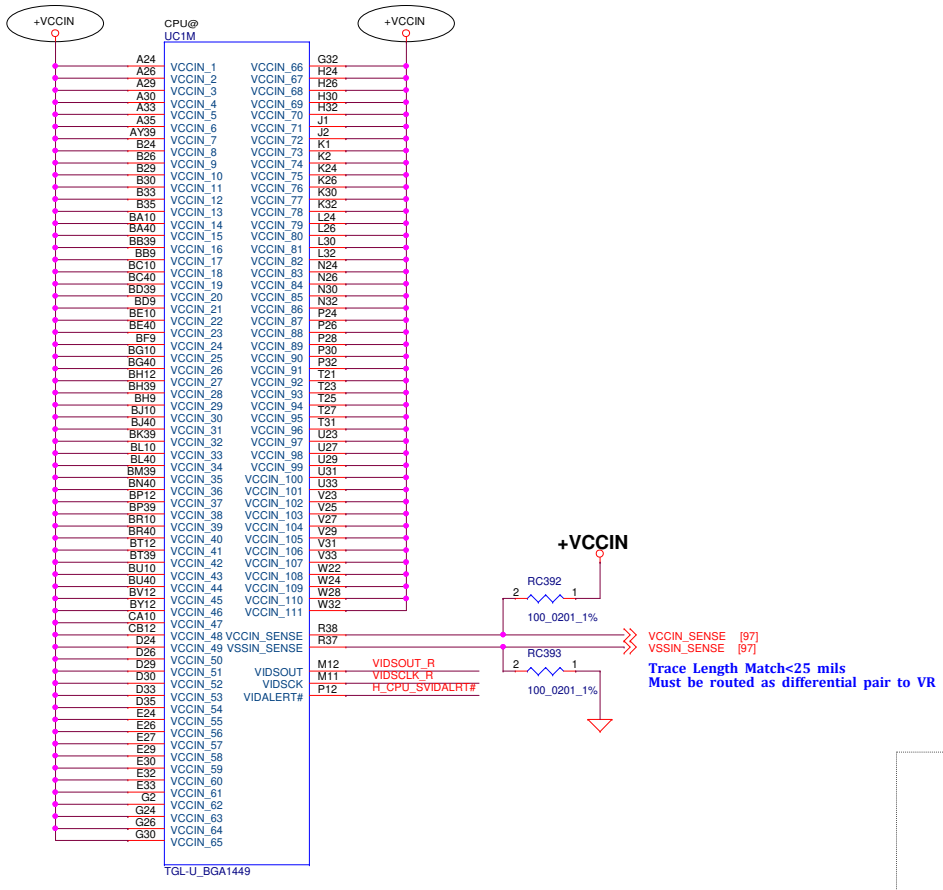
Compal Electronics, Inc.

Title: MCP(8/13)CSI,CNVi

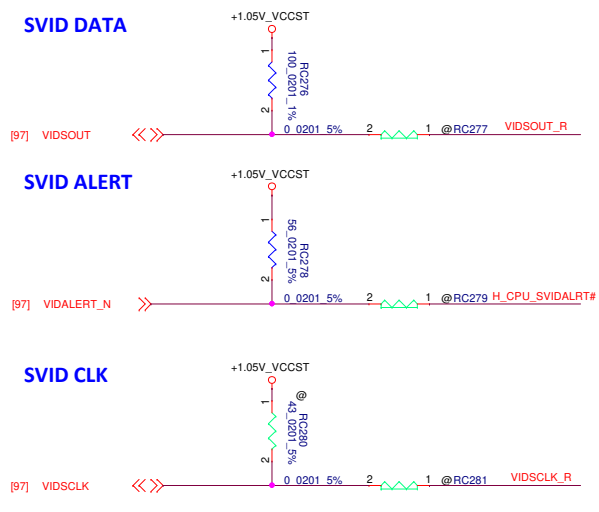
Size | Document Number: LA-K371P | Rev: 1.0

Date: Wednesday, October 28, 2020 | Sheet 13 of 125



Trace Length Match<25 mils
Must be routed as differential pair to VR

1.The total Length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
2.Route the Alert signal between the Clock and the Data signals.
CAD Note: Place the PU resistors close to CPU



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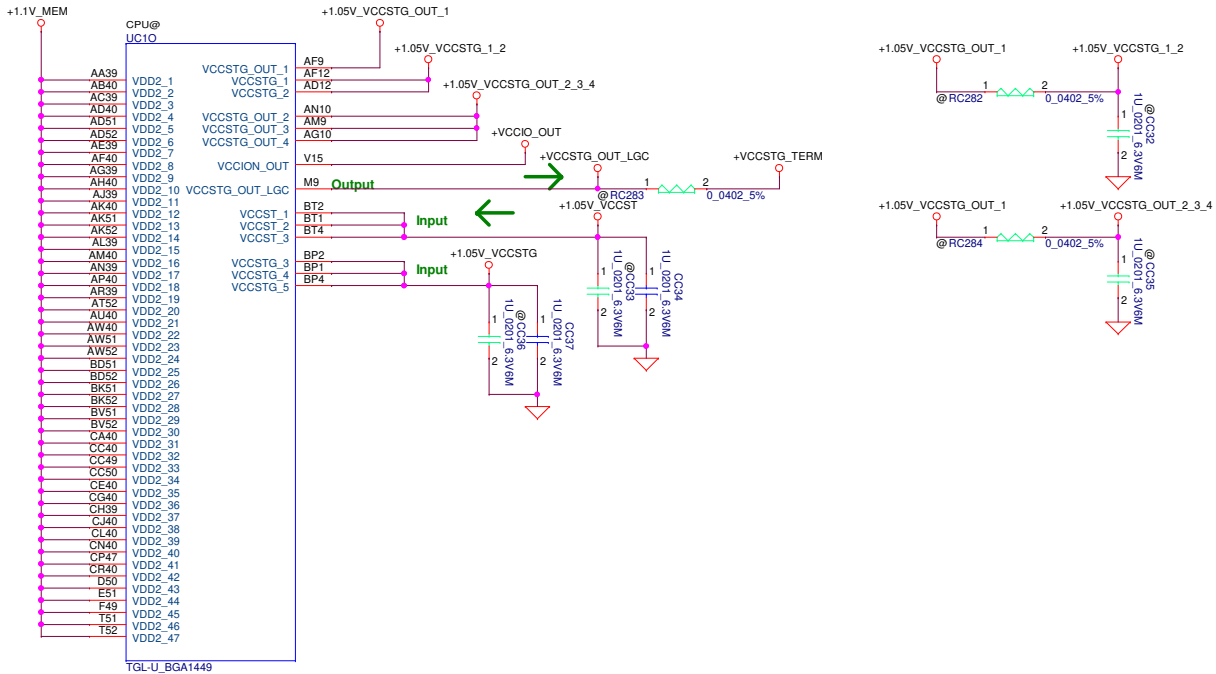
Compal Electronics, Inc.

Title: MCP(9/13)CPU PWR,SVID

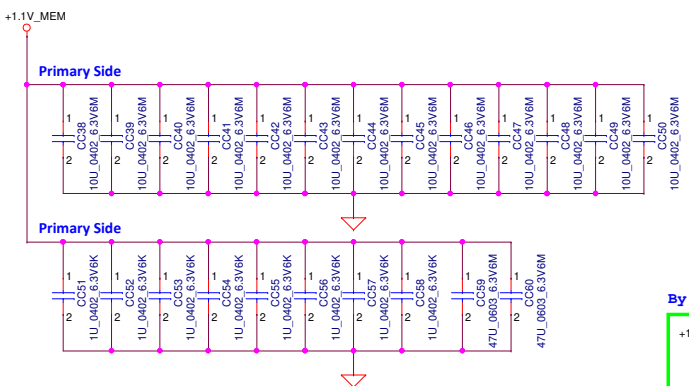
Size | Document Number: LA-K371P | Rev: 1.0

Date: Wednesday, October 28, 2020 | Sheet 14 of 125

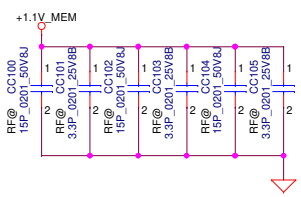
Refence 604917-tiger-lake-up3-processorline-bga-pkgballoutmechspec-rev1-6



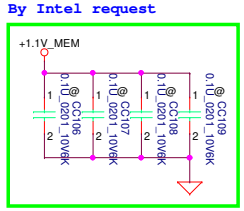
607872_TGL_UP3_PDG_Rev1p0.xlsx
TGL-UP3_8L_T3_SS_VDD2 sheet
VDD2:
Primary Side cap
2x 47uF 0603 + 8x 1uF 0402 + 13x 10uF 0402



RF CAPS - PLACE <4MM FROM SOC VDDQ, WITH EACH PAIR <12MM APART : EMC DDR RFI Mitigation



By Intel request



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Compal Electronics, Inc.

Title: MCP(10/13)CPU PWR

Size | Document Number: LA-K371P | Rev: 1.0

Date: Wednesday, October 28, 2020 | Sheet 15 of 125

+1.05V_VCCSTG source

SN74AUP1G97DRLR
FUNCTION TABLE

INPUTS C	B	A	OUTPUT Y
L	L	L	L
L	L	H	L
L	H	L	H
L	H	H	H
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	L

Confirm with Intel MIPI60 debug(pin# 17) POD_PRESENT2_N does not need to connect to VCCST/VCCSTG power override?

+1.05V_VCCST source

Confirm with Intel MIPI60 debug(pin# 17) POD_PRESENT2_N does not need to connect to VCCST/VCCSTG power override?

SN74AUP1G97DRLR
FUNCTION TABLE

INPUTS C	B	A	OUTPUT Y
L	L	L	L
L	L	H	L
L	H	L	H
L	H	H	H
H	L	L	L
H	L	H	H
H	H	L	L
H	H	H	L

Place capacitor close to CPU pin

Place capacitor close to CPU pin

Place capacitor close to CPU pin

Cancel reservation for 1.8V cause of Codec is 3.3V

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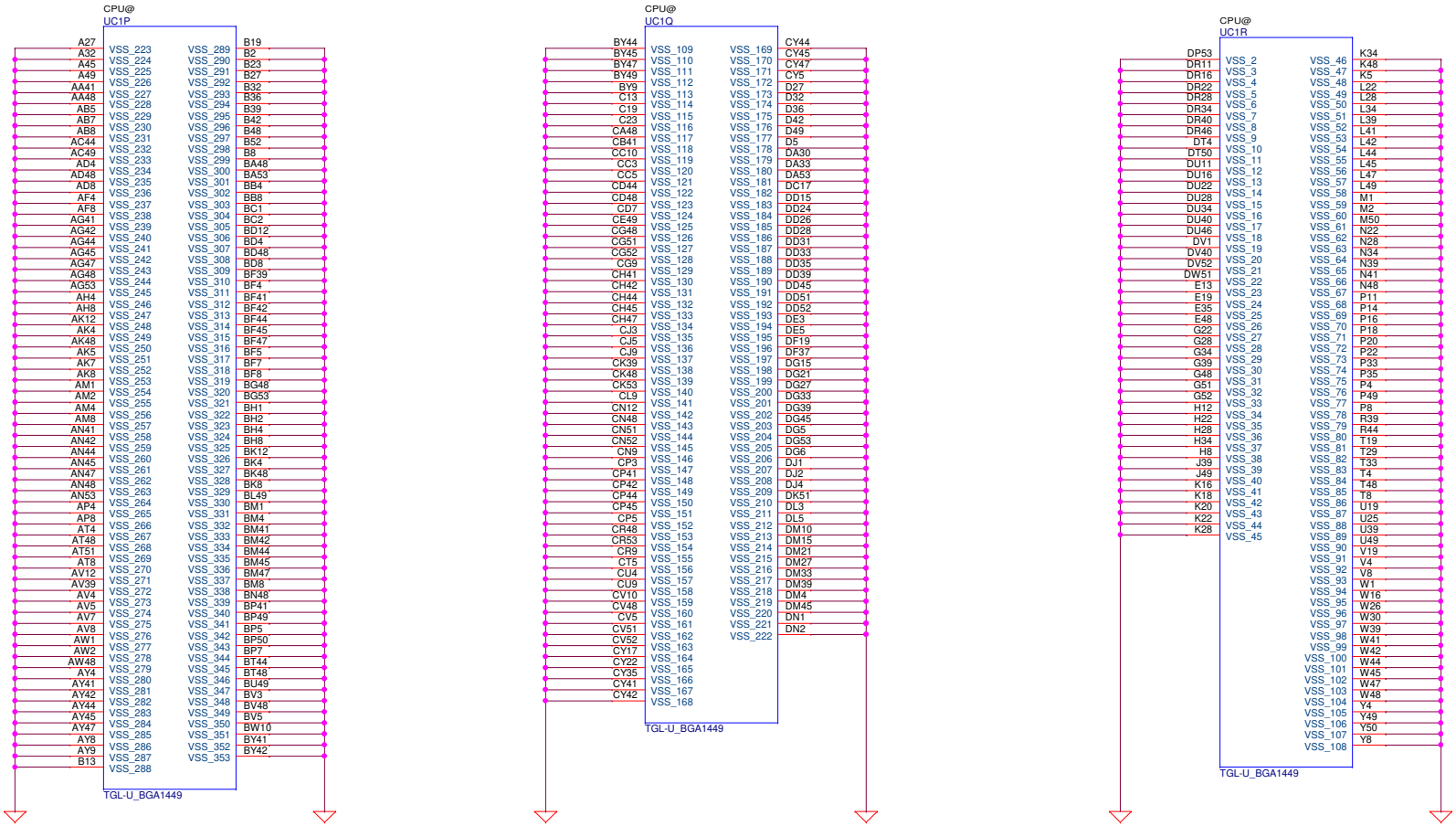
Compal Electronics, Inc.
Title: MCP(11/13)PCH Power
Size: Document Number: LA-K371P
Rev: 1.0
Date: Wednesday, October 28, 2020
Sheet 16 of 125



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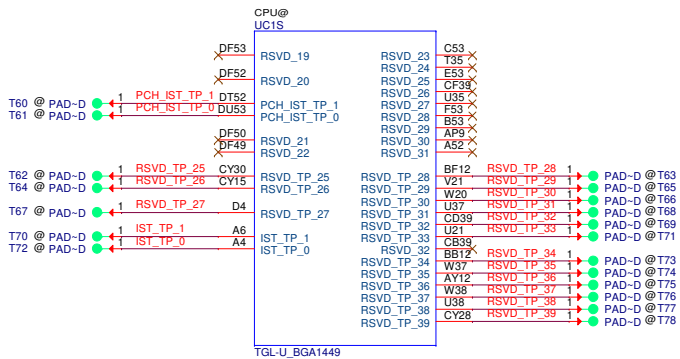
Compal Electronics, Inc.

Title: MCP(12/13)VSS

Size | Document Number: LA-K371P | Rev: 1.0

Date: Wednesday, October 28, 2020 | Sheet 17 of 125



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Compal Electronics, Inc.

Title: MCP(13/13)RSVD

Size | Document Number: LA-K371P | Rev: 1.0

Date: Wednesday, October 28, 2020 | Sheet 18 of 125

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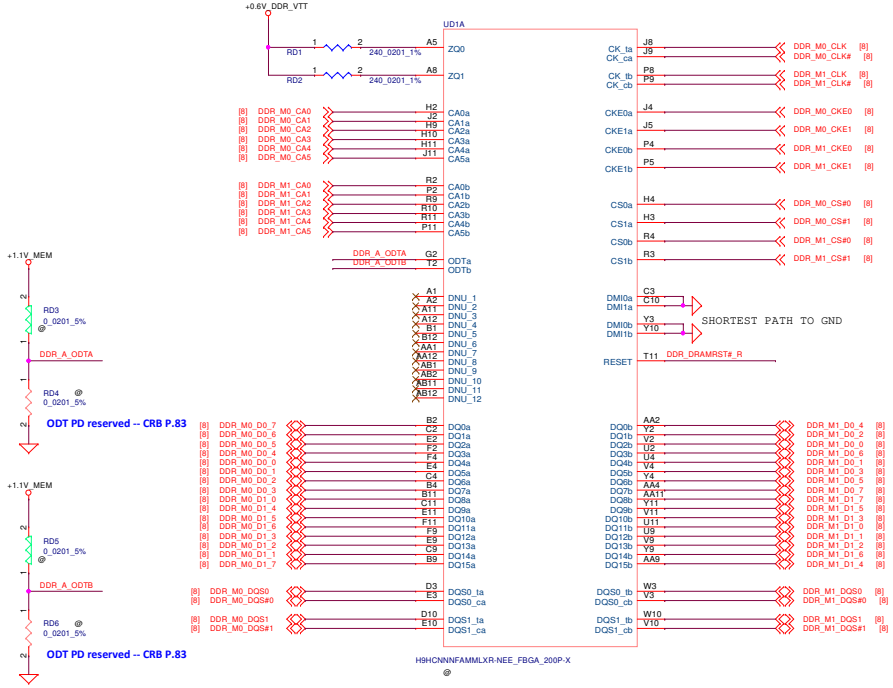
LPDDR4x_A (0,1)



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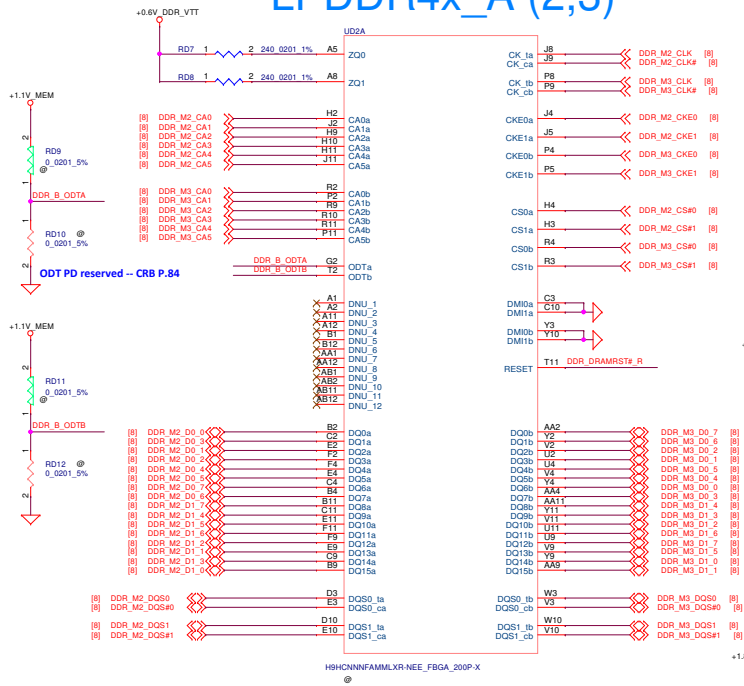
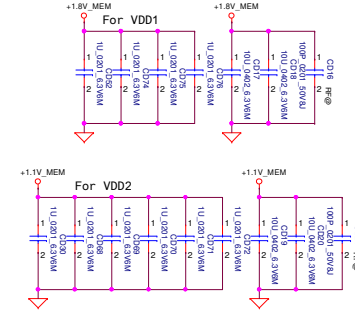


For UD1



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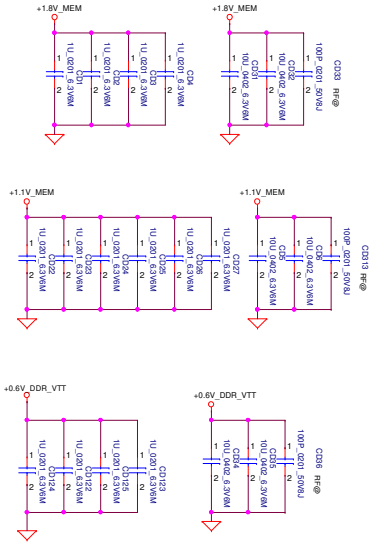

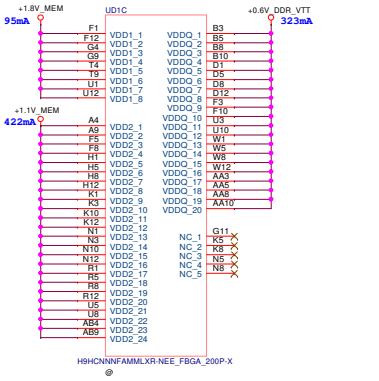

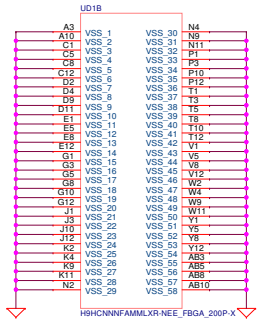

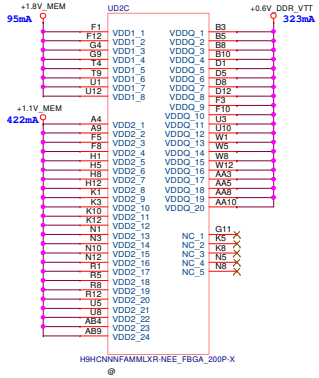

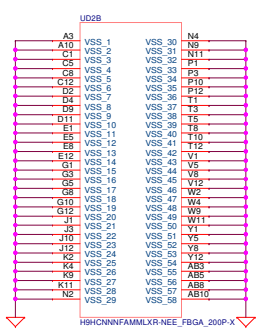

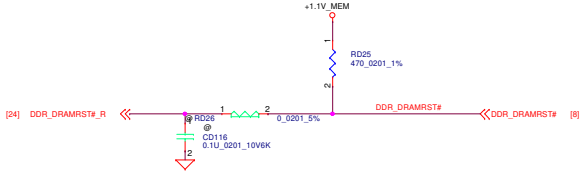

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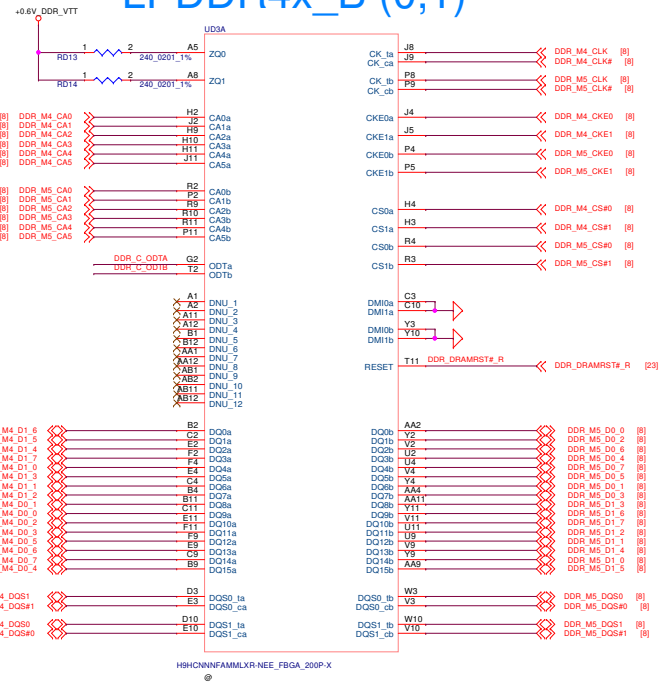
Compal Electronics, Inc.

Title: DDR4 DIMMA

Size: Document Number: LA-K371P Rev: 1.0

Date: Wednesday, October 28, 2020 Sheet 23 of 125

LPDDR4x_B (0,1)



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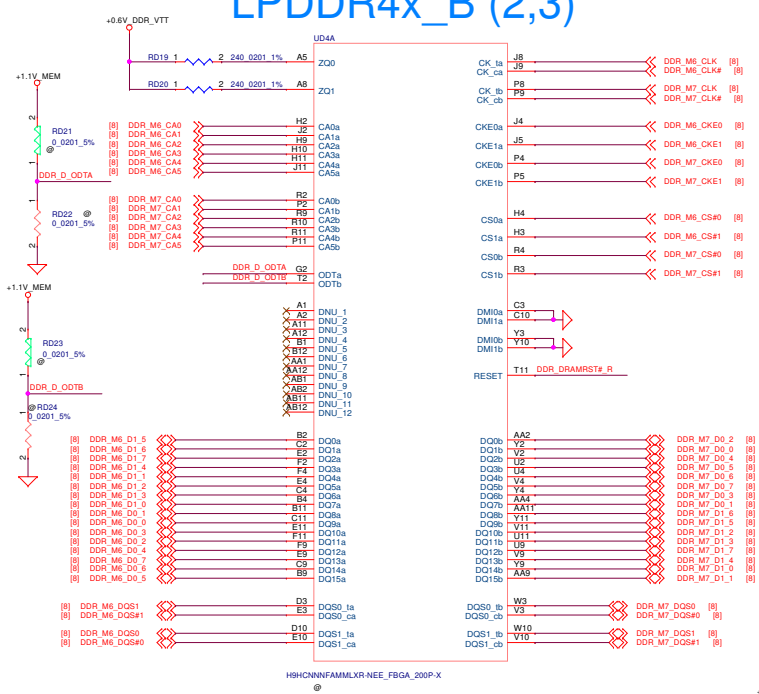
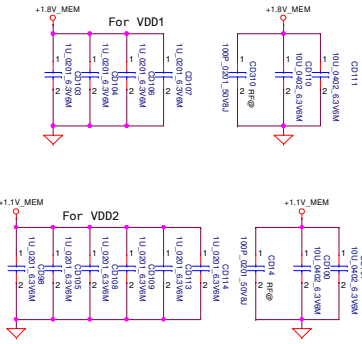
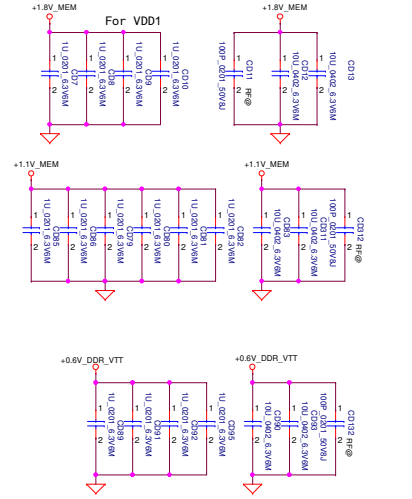
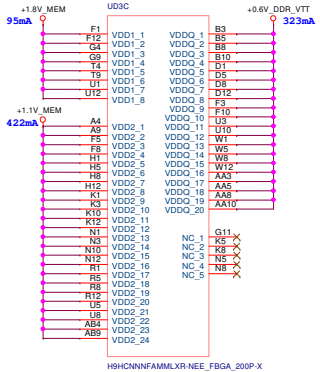


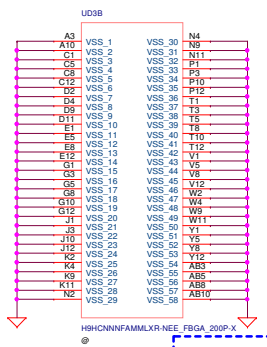
For UD3

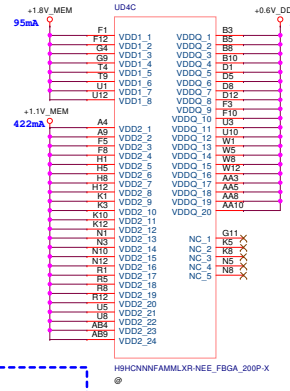


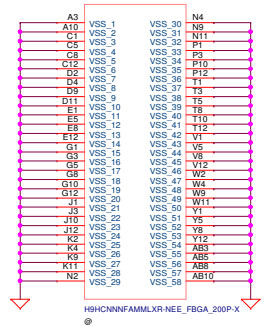
For UD4

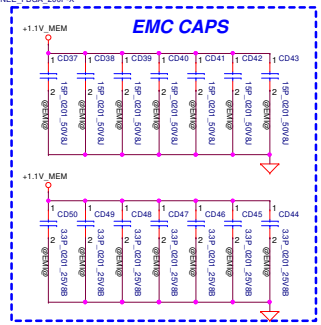












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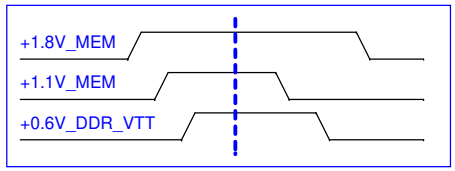
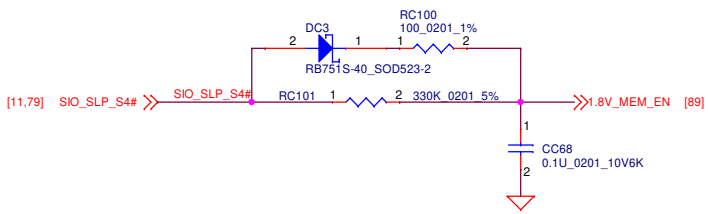
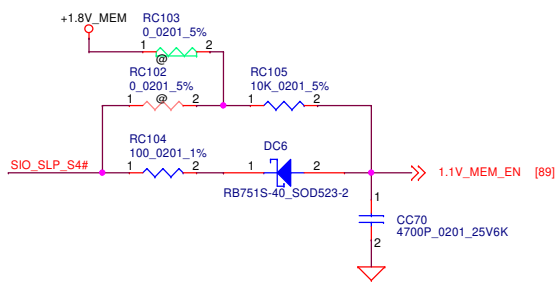
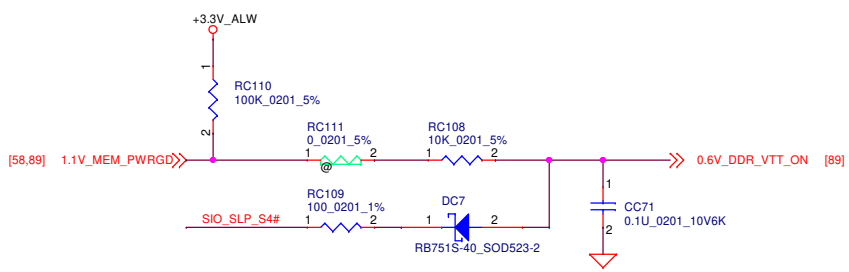
Follow Intel RVP for LP4x sequence









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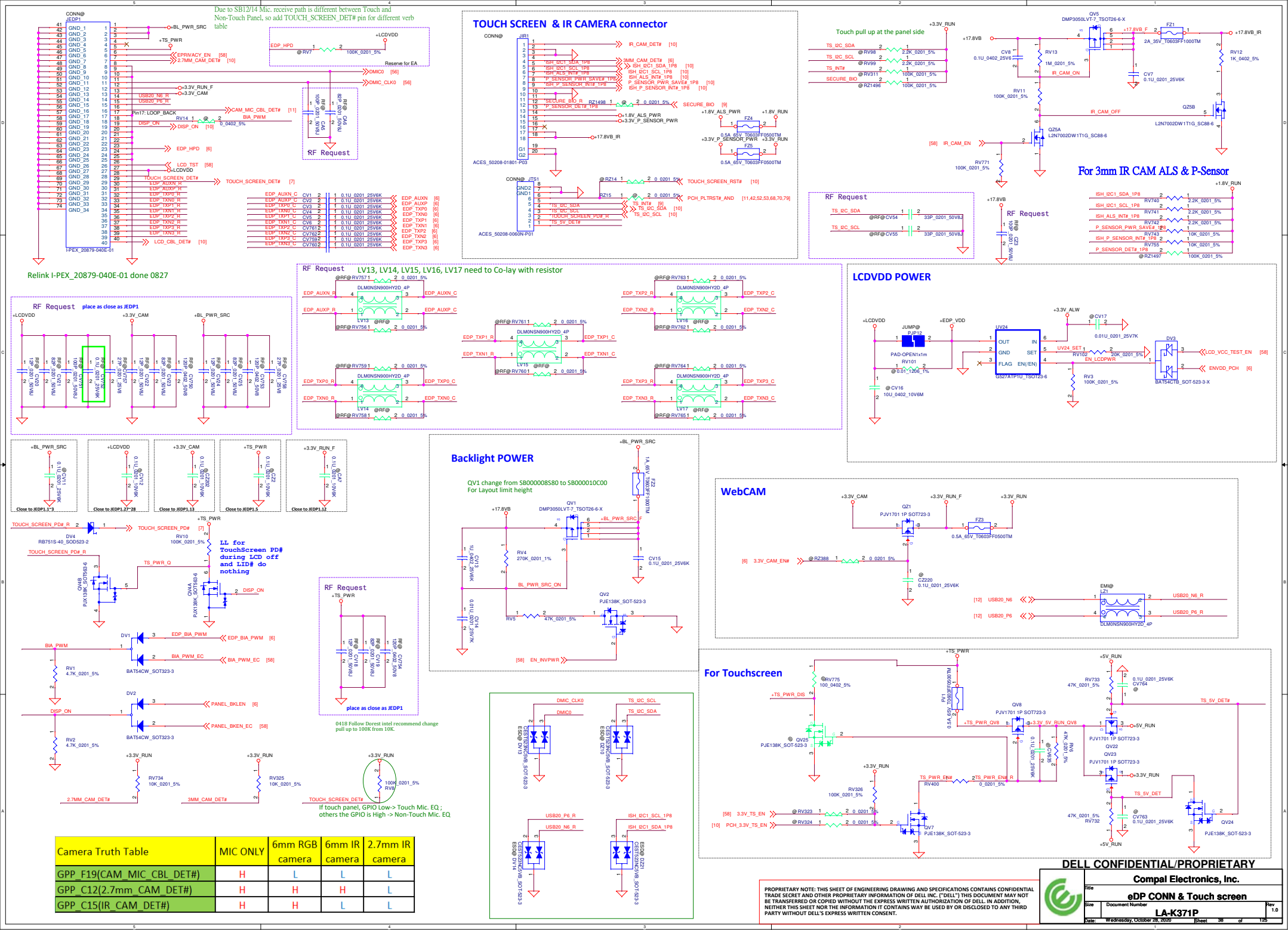

Camera Truth Table	MIC ONLY	6mm RGB camera	6mm IR camera	2.7mm IR camera
GPP_F19(CAM_MIC_CBL_DET#)	H	L	L	L
GPP_C12(2.7mm_CAM_DET#)	H	H	H	L
GPP_C15(IR_CAM_DET#)	H	H	L	L

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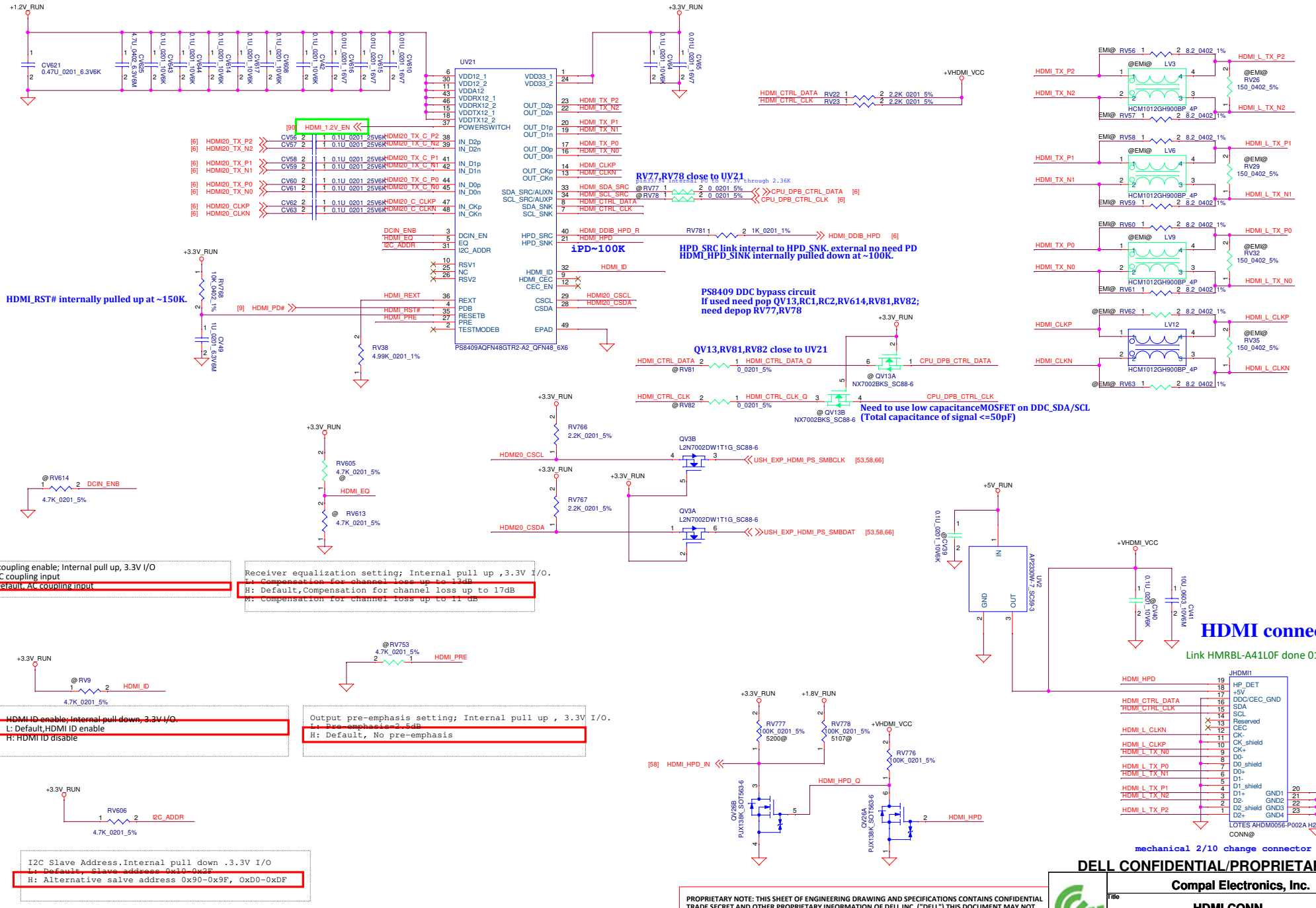

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Title	CRT	
Size	Document Number: LA-K371P	Rev: 1.0
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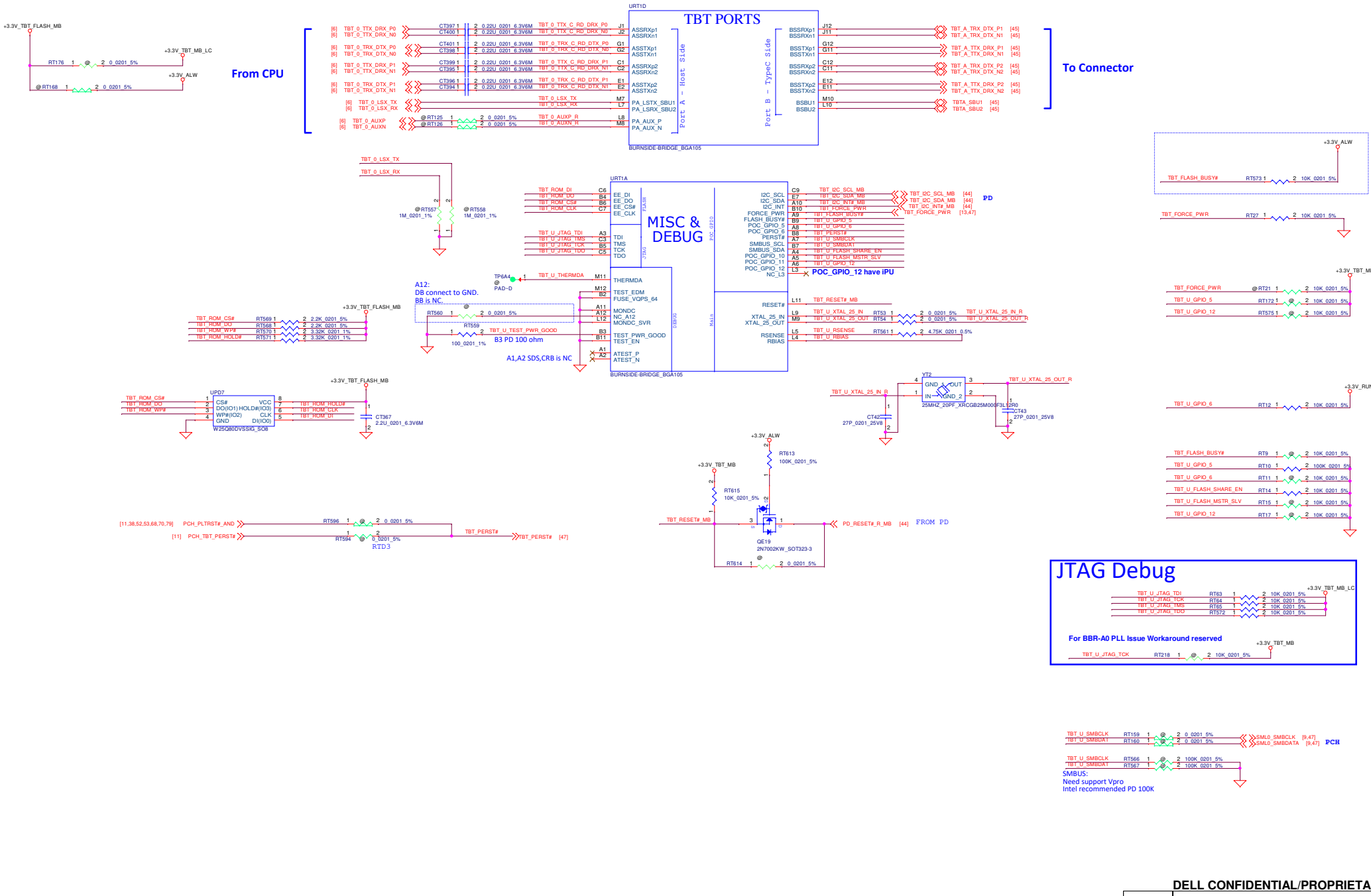
From CPU
TBT PORTS
URT1D
BURNSIDE-BRIDGE_BGA105
Port B - TypeC Side
Port A - Host Side
To Connector
URT1A
MISC & DEBUG
BURNSIDE-BRIDGE_BGA105
A12:
DB connect to GND.
BB is NC.
B3 PD 100 ohm
A1,A2 SDS,CRB is NC
POC_GPIO_12 have iPU
PD
UPD7
W25Q80DVSSIG_SO8
RTD3
FROM PD
JTAG Debug
For BBR-A0 PLL Issue Workaround reserved
SMBUS:
Need support Vpro
Intel recommended PD 100K
PCH
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Compal Electronics, Inc.
TBT-BB-(1/2) TCSS
LA-K371P
Wednesday, October 28, 2020
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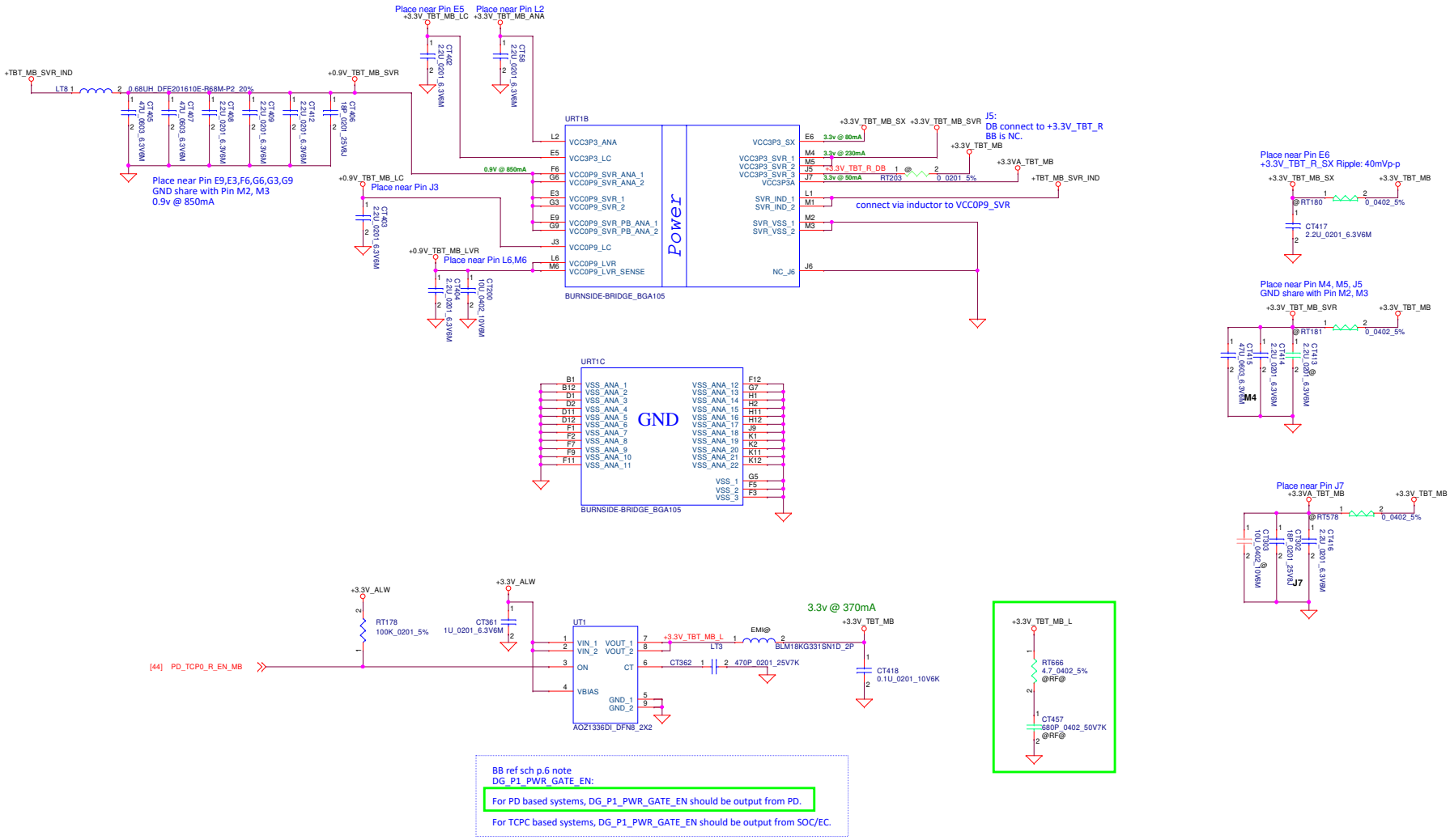

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Title	TBT-AR-SP(2/2) VCC/VSS
Size	Document Number: LA-K371P
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Date:	Wednesday, October 28, 2020
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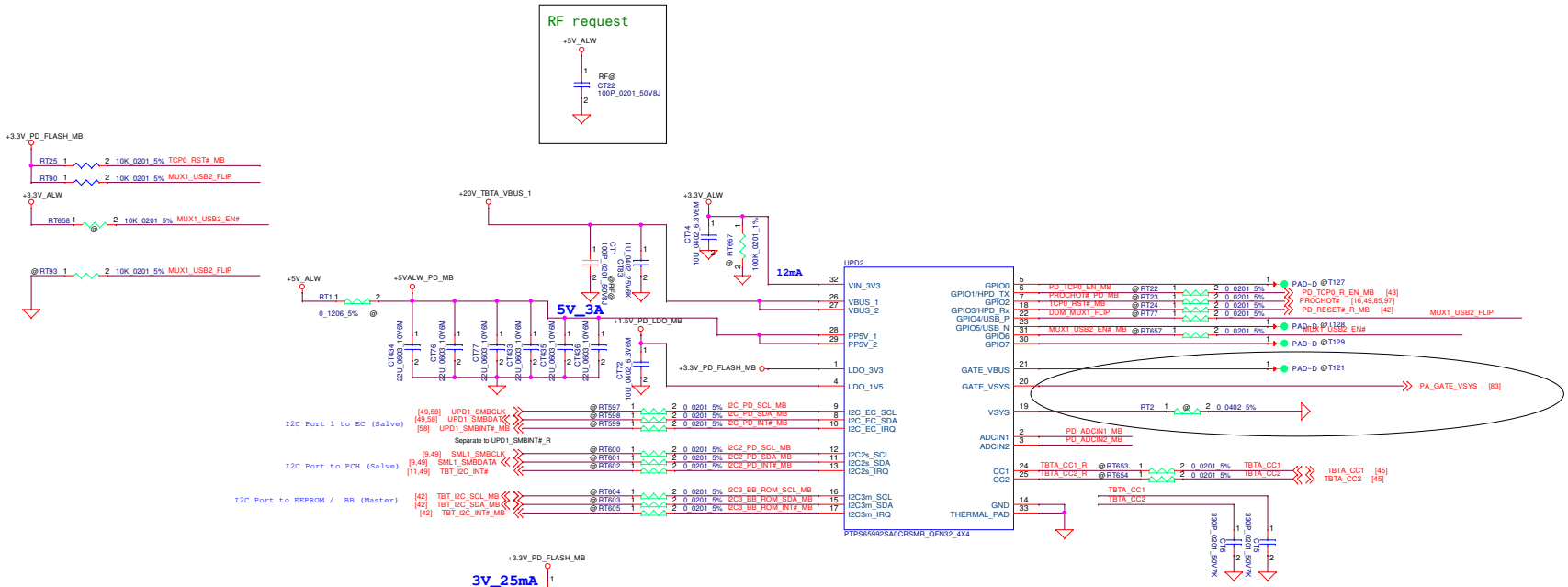


Table 2. Decoding of ADCIN1 and ADCIN2 Pins

DIV = R_{Rdown} / (R_{Up} + R_{Rdown})[1]		Without using R_{Up} or R_{Rdown}	ADCINx decoded value
MIN	MAX		
0	0.0228	tie to GND	1
0.0229	0.0722	N/A	2
0.0723	0.1425	N/A	3
0.1426	0.2372	N/A	4
0.2373	0.3671	N/A	5
0.3672	0.7064	tie to LDO_1V5	6
0.7065	0.9060	N/A	8
0.9061	1.0	tie to LDO_3V3	7

(1) External resistor tolerance of 1% is recommended. Resistor values must be chosen to yield a DIV value centered nominally between listed MIN and MAX values.

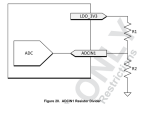


Table 5. I²C Default Slave Address for I2C_EC_SCL/SDA.

I²C address index (decoded from ADCIN1 and ADCIN2)[1]	Port	Slave Address								Available During BOOT
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
#1	A	0	1	0	0	0	0	0	R/W	Yes
#2	A	0	1	0	0	0	0	1	R/W	Yes
#3	A	0	1	0	0	0	1	0	R/W	Yes
#4	A	0	1	0	0	0	1	1	R/W	Yes

Table 6. Device Configuration using ADCIN1 and ADCIN2

ADCIN1 decoded value [1]	ADCIN2 decoded value [1]	I²C address Index [2]	Dead Battery Configuration
7	5	#1	AlwaysEnableSink: The device always enables the sink path regardless of the amount of current the attached source is offering. USB PD is disabled until configuration is loaded.
5	5	#2	
5	6	#3	
1	7	#4	
7	4	#1	SinkRequires_3.0A: The device only enables the sink path if the attached source is offering at least 3.0A. USB PD is disabled until configuration is loaded.
4	4	#2	
3	0	#3	
2	7	#4	
7	6	#1	SinkRequires_1.5A: The device only enables the sink path if the attached source is offering at least 1.5A. USB PD is disabled until configuration is loaded.
6	6	#2	
6	5	#3	
6	7	#4	
7	3	#1	NegotiateHighVoltage: The device always enables the sink path during the initial implicit contract regardless of the amount of current the attached source is offering. The PD controller will enter the 'APP ' mode, enable USB PD PHY and negotiate a contract for the highest power contract that is offered up to 20 V.
3	3	#2	
4	0	#3	
3	7	#4	
7	0	#1	SafeMode: The device does not enable he sink path. USB PD is disabled until configuration is loaded. Note that the configuration could put the device into a source-only mode.
0	0	#2	
6	0	#3	
5	7	#4	

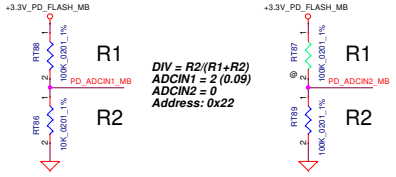
Table 4. Function table[1]

Input		Channel
S	OE	
L	L	D+ = 1D+; D- = 1D-
H	L	D+ = 2D+; D- = 2D-
X	H	switches off

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.

ADCIN1_PD:100K/10K = 0.09

ADCIN2_PD:NC/100K = 0



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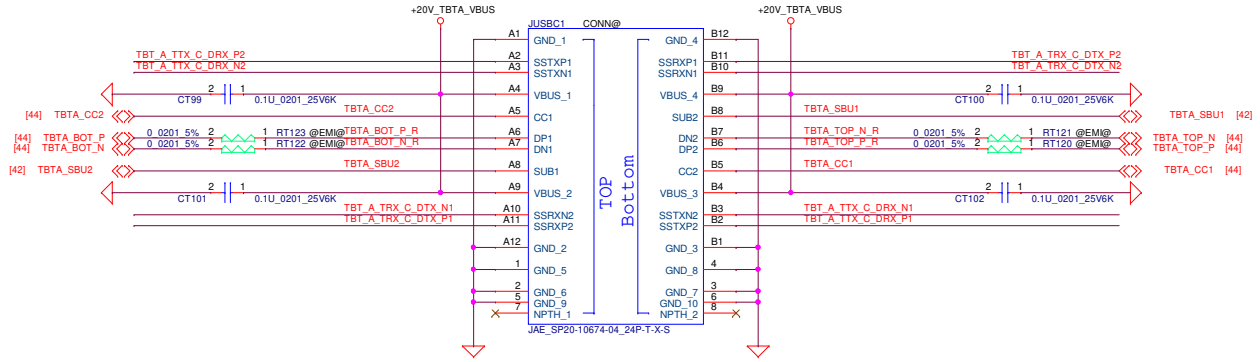
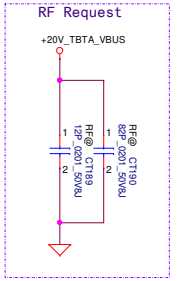
Compal Electronics, Inc.

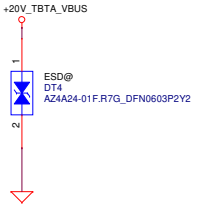
Title: [Type C]PD Controller TI

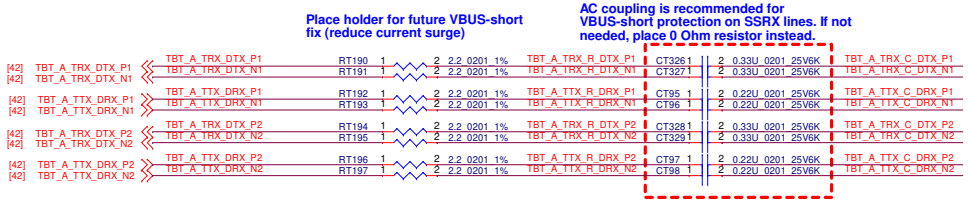
Size | Document Number: LA-K371P | Rev: 1.0

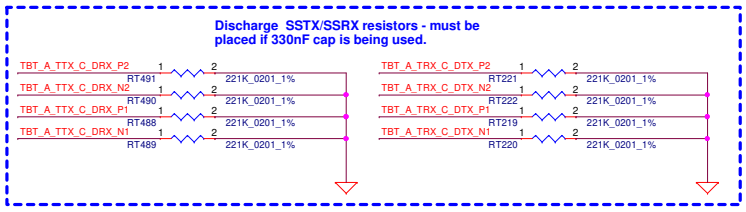
Date: Wednesday, October 28, 2020 | Sheet 44 of 125

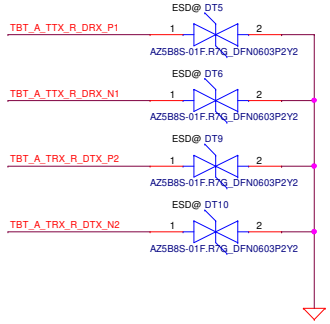


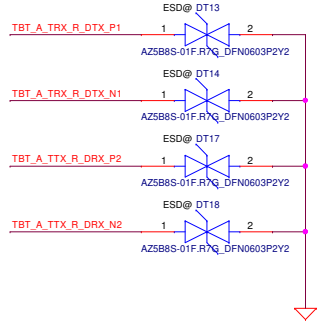


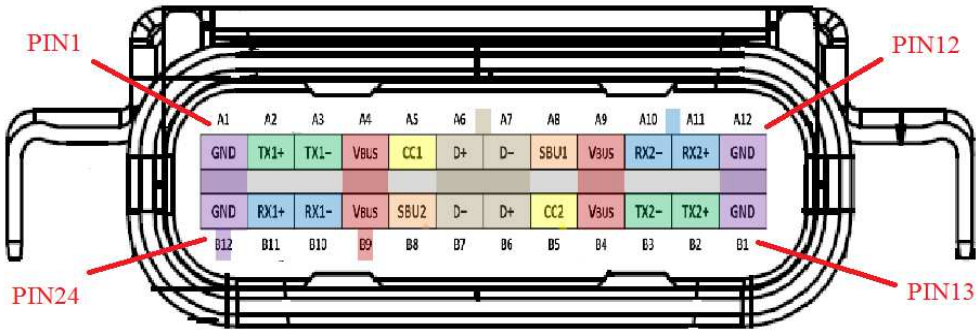


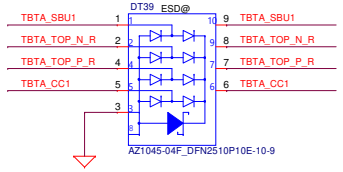


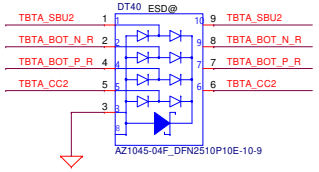












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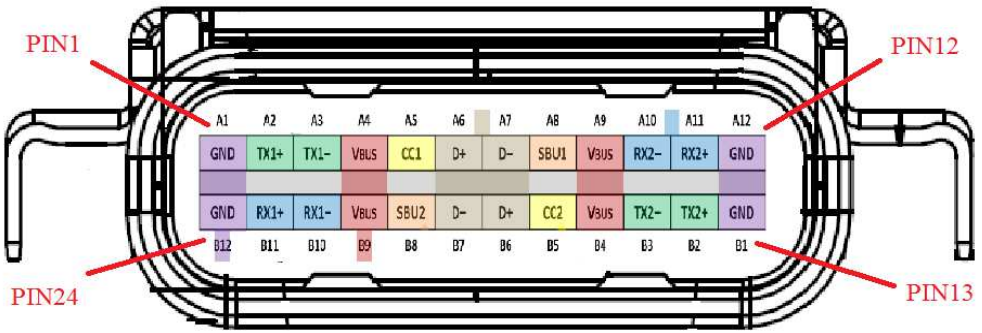
Move to TBT Daughter Board



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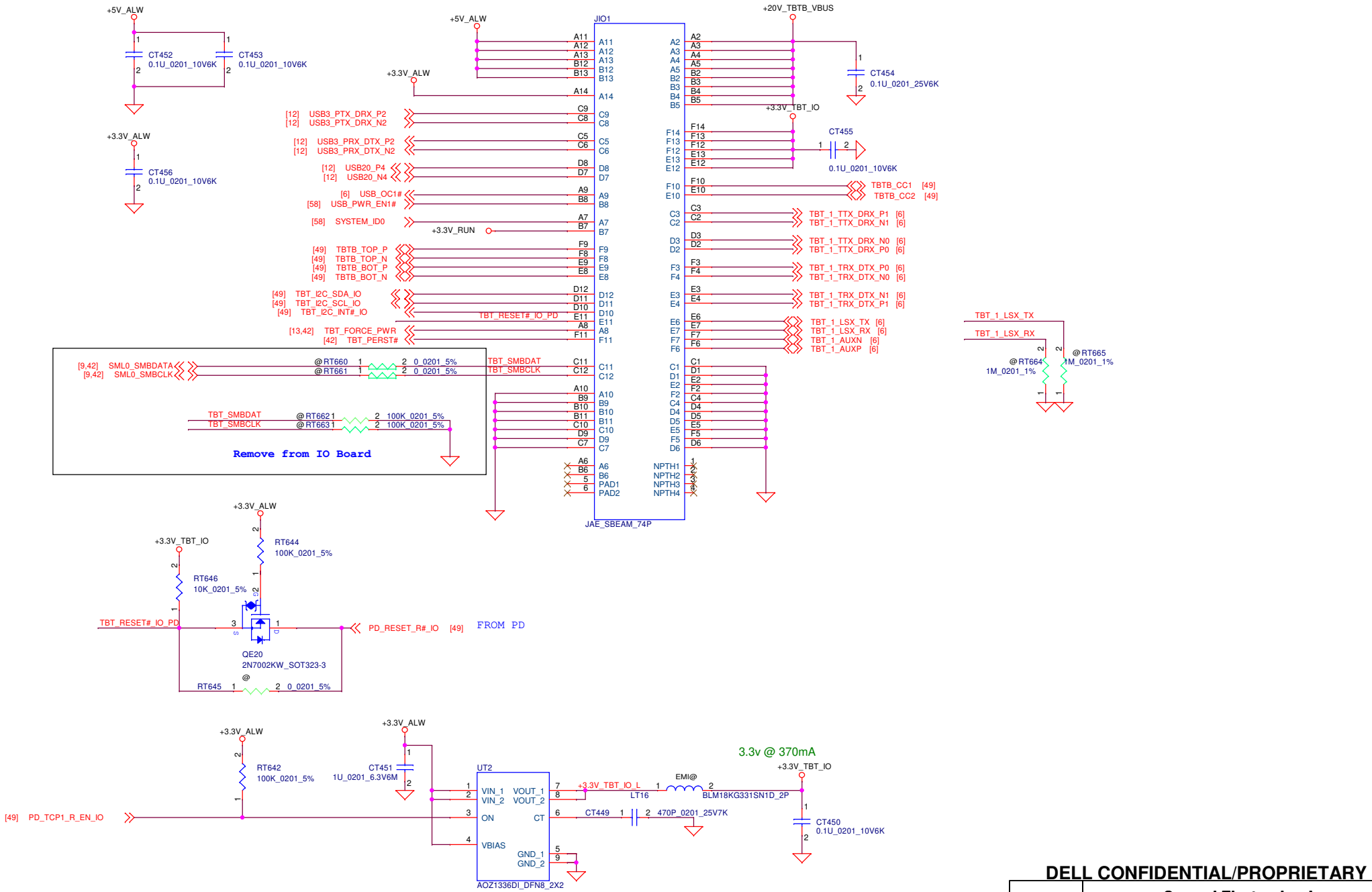

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Title: **TYPE-C_Port3 (1/2)**

Size | Document Number: **LA-K371P** | Rev: 1.0

Date: Wednesday, October 28, 2020 | Sheet 48 of 125

+20V_TBTB_VBUS_1

2020/2/25 update to 992SAD

12mA

5V_3A

UPD4

PTPS65992SA0CRSMR_QFN32_4X4

I2C Port 1 to EC (Salve)

I2C Port to PCH (Salve)

I2C Port to EEPROM / BB (Master)

UPD5

CAT24C256WI?GT3 SOIC 8P

Table 1. Enable and Disable Function Table

ENA	ENB	INA	INB	OUTA0	OUTA1	OUTB0	OUTB1
0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
0	1	Hi-Z	Enabled	Hi-Z	Hi-Z	Enabled	Enabled
1	0	Enabled	Hi-Z	Enabled	Enabled	Hi-Z	Hi-Z
1	1	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled

Table 6. Complete Function Table

SAI	SBI	SA0	SBO	OUTA0	OUTA1	OUTB0	OUTB1	FUNCTIONAL MODE
0	0	0	0	INB	—	INA	—	Crosspoint, 1-channel 1:4 mux
0	0	0	1	INB	—	—	INA	1-channel 1:4 mux
0	0	1	0	—	INB	INA	—	1-channel 1:4 mux
0	0	1	1	—	INB	—	INA	1-channel 1:4 mux
0	1	0	0	INB	—	INA	—	
0	1	0	1	INB	—	—	INA	
0	1	1	0	—	INB	INB	—	
0	1	1	1	—	INB	—	INB	
1	0	0	0	INA	—	INA	—	Fan-out 1:2 configuration
1	0	0	1	INA	—	—	INA	Fan-out 1:2 configuration
1	0	1	0	—	INA	INA	—	Fan-out 1:2 configuration
1	0	1	1	—	INA	—	INA	Fan-out 1:2 configuration
1	1	0	0	INA	—	INB	—	Crosspoint, 2-channel 1:2 mux, 1-channel 1:4 mux
1	1	0	1	INA	—	—	INB	2-channel 1:2 mux,1-channel 1:4 mux
1	1	1	0	—	INA	INB	—	2-channel 1:2 mux,1-channel 1:4 mux
1	1	1	1	—	INA	—	INB	2-channel 1:2 mux,1-channel 1:4 mux

USB only on TBTA_TOP_P/N;TBTB_TOP_P/N

USB on TBTA_TOP_P/N;TBTB_TOP_P/N
DDM on TBTA_BOT_P/N;TBTB_BOT_P/N

USB only on TBTA_BOT_P/N;TBTB_BOT_P/N

USB on TBTA_BOT_P/N;TBTB_BOT_P/N
DDM on TBTA_TOP_P/N;TBTB_TOP_P/N

Table 6. Device Configuration using ADCIN1 and ADCIN2 .

ADCIN1 decoded value (1)	ADCIN2 decoded value (1)	I²C address Index (2)	Dead Battery Configuration
7	5	#1	AlwaysEnableSink: The device always enables the sink path regardless of the amount of current the attached source is offering. USB PD is disabled until configuration is loaded.
6	6	#2	
5	0	#3	
1	7	#4	

Table 2. Decoding of ADCIN1 and ADCIN2 Pins

DIV = R_{DOWN} / (R_{UP} + R_{DOWN})(1)		Without using R_{UP} or R_{DOWN}	ADCINx decoded value
MIN	MAX		
0	0.0228	tie to GND	0
0.0229	0.0722	N/A	1
0.0723	0.1425	N/A	2
0.1425	0.2372	N/A	3
0.2373	0.3671	N/A	4
0.3672	0.7064	tie to LDO_1V5	5
0.7065	0.9060	N/A	6
0.9061	1.0	tie to LDO_3V3	7

(1) External resistor tolerance of 1% is recommended. Resistor values must be chosen to yield a DIV value centered nominally between listed MIN and MAX values.

Table 5. I²C Default Slave Address for I2C_EC_SCL/SDA.

I²C address index (decoded from ADCIN1 and ADCIN2)(1)	Port	Slave Address								Available During BOOT
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
#1	A	0	1	0	0	0	0	0	R/W	Yes
#2	A	0	1	0	0	0	0	1	R/W	Yes
#3	A	0	1	0	0	0	1	0	R/W	Yes
#4	A	0	1	0	0	0	1	1	R/W	Yes

ADCIN1_PD:100K/nc = 1

ADCIN2_PD:100K/100K = 0.5

DIV = R2/(R1+R2)
ADCIN1 = 7 (1)
ADCIN2 = 5 (0.5)
Address: 0x20

UPD6

TS3DS10224RUKR_WQFN20_3X3-X

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Size: Document Number: LA-K371P
Rev: 1.0
Date: Wednesday, October 28, 2020
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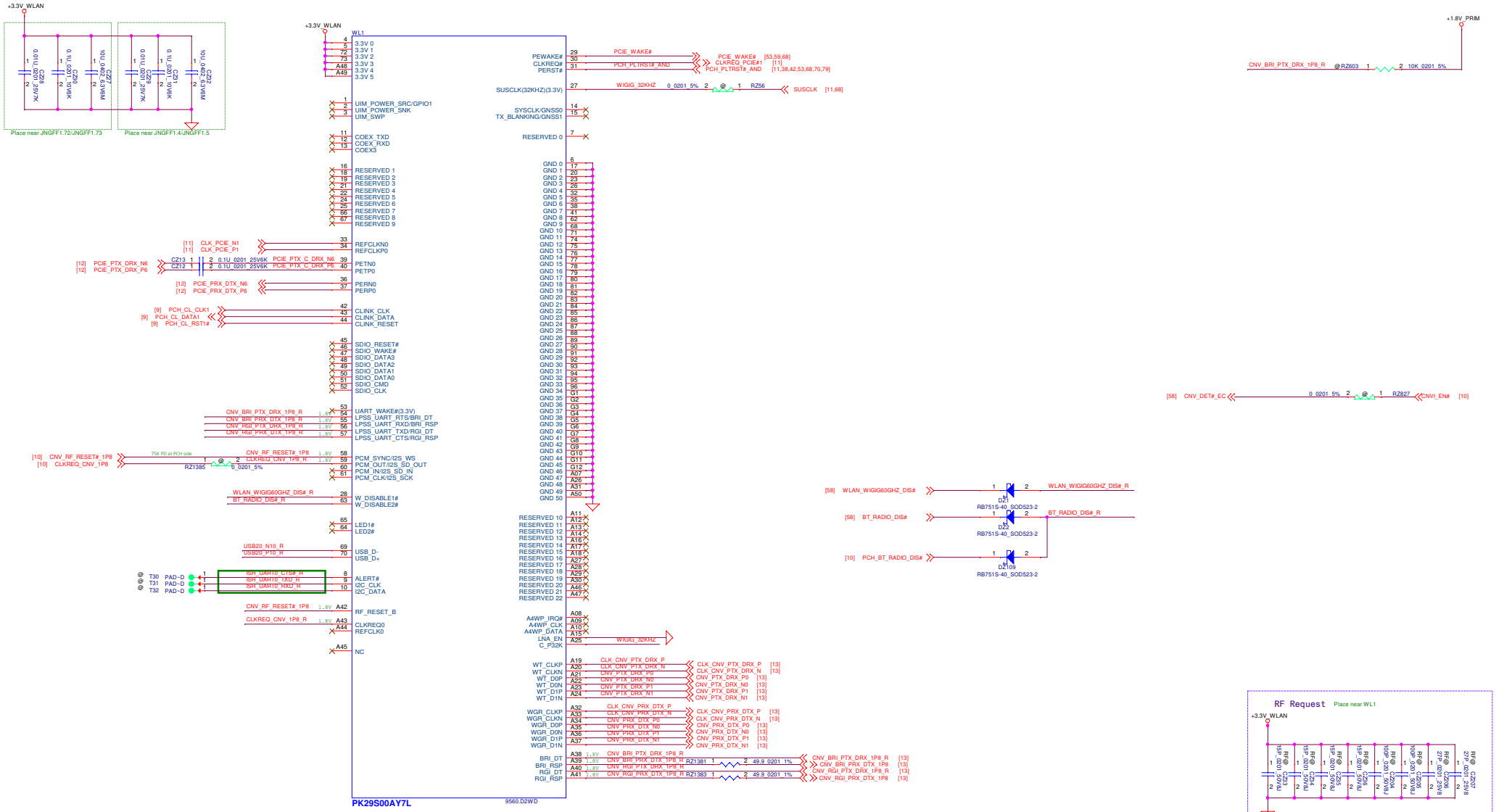

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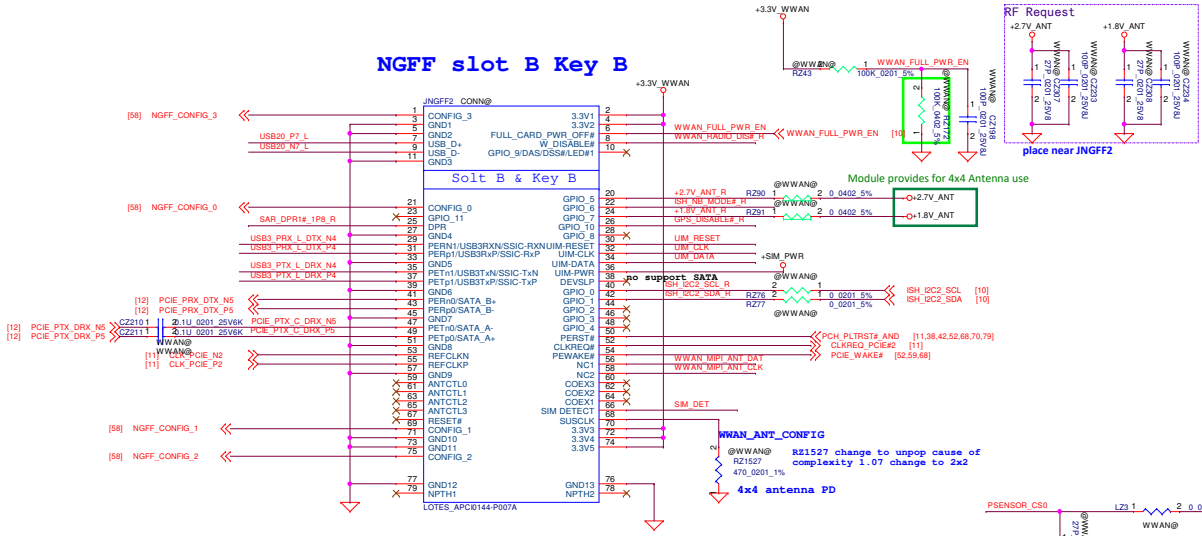
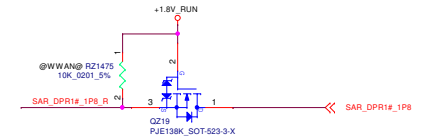
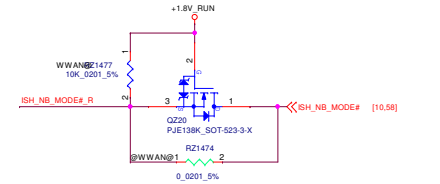
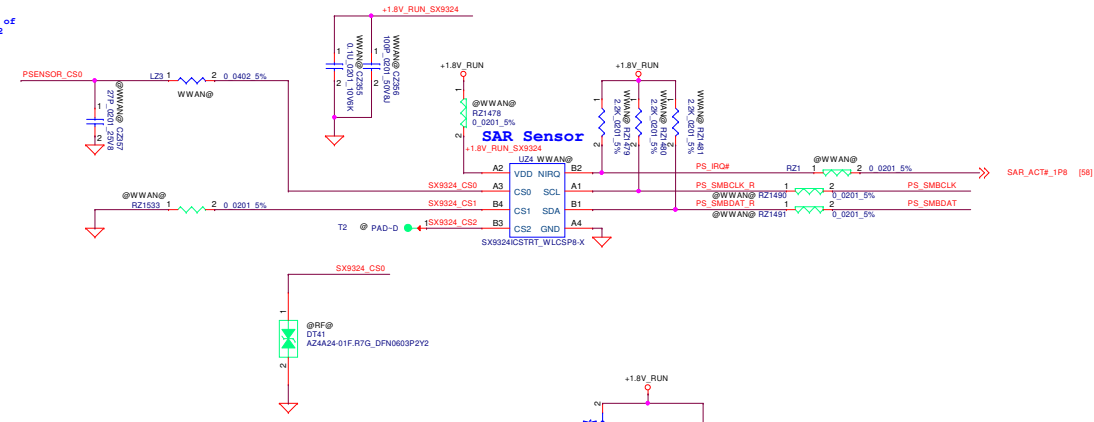
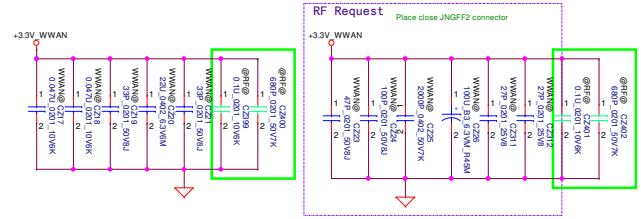
NGFF slot B Key B

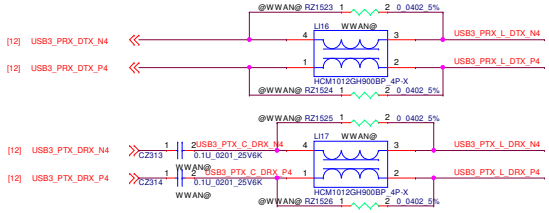


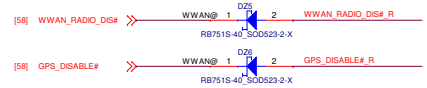


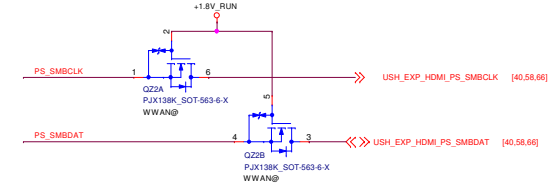




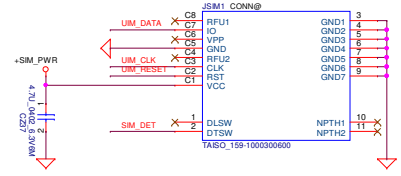


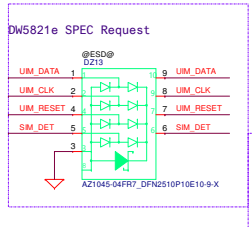


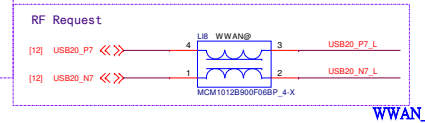


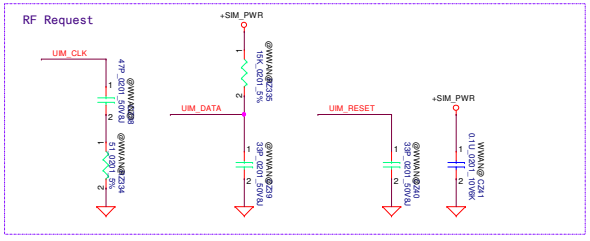


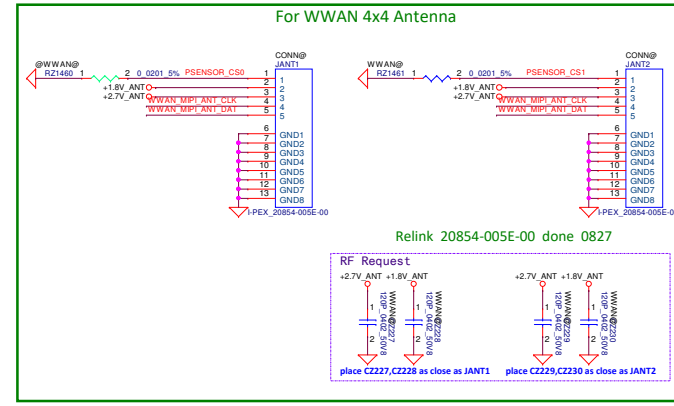
SIM Card











WWAN_MIPI_ANT_DAT and WWAN_MIPI_ANT_CLK
(1)The trace length < 30cm
This max length guidance is practical level of definition.
(2)Spacing to all other signal need 4x line width

STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type	M3042_PCIE#_SATA
	GND	GND	GND	GND	SSD-SATA	High
	GND	HIGH	GND	GND	SSD-PCIE(2 lane)	Low
	HIGH	GND	GND	GND	WWAN	Low
14	HIGH	GND	HIGH	HIGH	HCA-PCIE(1 lane)	Low
15	HIGH	HIGH	HIGH	HIGH	NA	Low

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1W x 1ch, 4ohm (Transducer spec is 8Ohm/0.5Watt per unit, there are two transducer units in one speaker box.)

Internal Speakers Header

40 mils trace keep 20 mil spacing

Link ACES_50278-00801-001 DONE 0809

Smart Amp Vendor	Vendor1 FG	Vendor2 Zylux	Vendor3 VECO
SMART_SPK_DET0# (PCH_GPP_B15)	High	Low	High
SMART_SPK_DET1# (PCH_GPP_C23)	High	High	Low

Close to UA1

Close to UA1 pin14

Close to UA1 pin5

Place closely to Pin 48.

Add for solve pop noise and detect issue

HDA_Link is 3.3V,no need level shift circuit

Place CA29/CA76 close to Codec

0809 change to 1U 0201*2 for MLCC shortage only Samsung,Taiyo,Murata can use

Place CA49/CA77 close to Codec

Power sequence +5V_RUN_AUDIO(501us) > +3.3V_RUN_AUDIO(1204 us) > +1.5V_RUN

500mA

PU on Sub Board

Add this Filter to avoid other components/chips be influenced

HP-Out-Right

HP-Out-Left

Nokia-MIC

iPhone-MIC

Universal Jack

Global Headset

Normal Open

RF Request

+3.3V_ALW

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Codec ALC3254

Size: Document Number: LA-K371P

Rev: 1.0

Date: Wednesday, October 28, 2020

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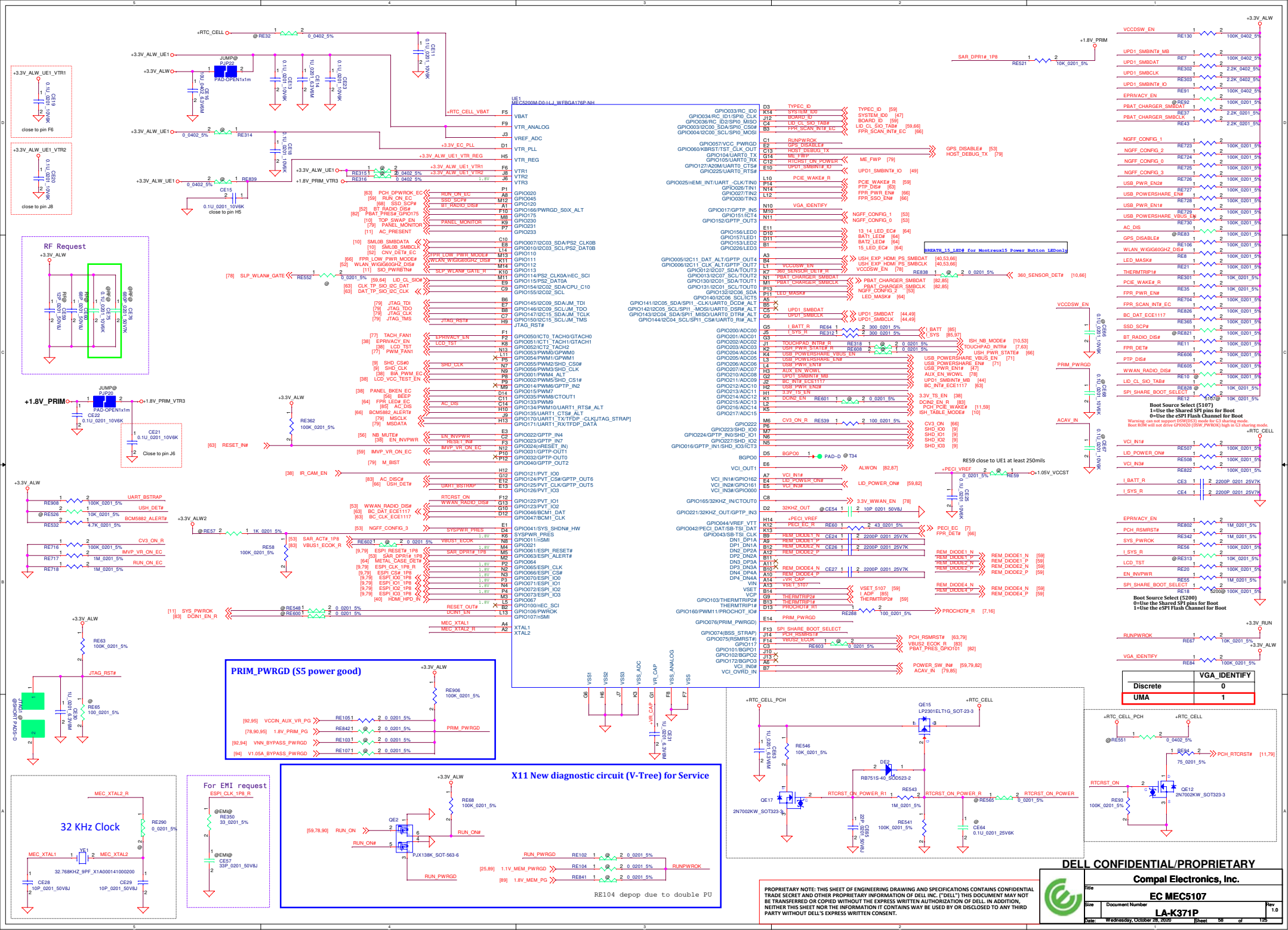
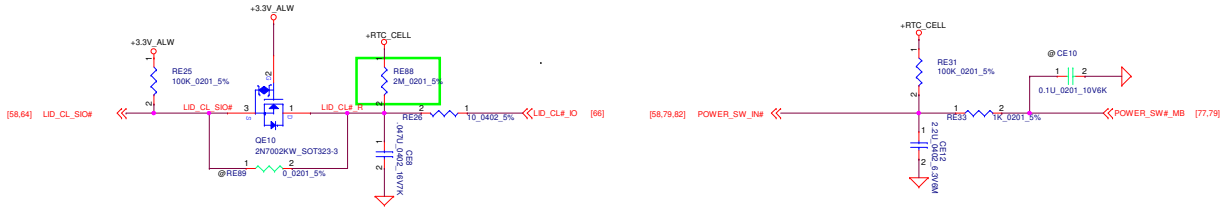


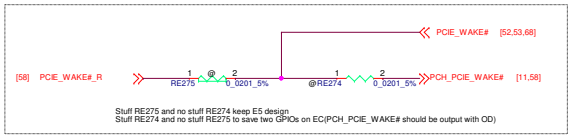
	VGA_IDENTIFY
Discrete	0
UMA	1

Boot Source Select (5107)
1=Use the Shared SPI pins for Boot
0=Use the eSPI Flash Channel for Boot
Warning: can not support DSW(DS3) mode for G3 sharing mode.
Boot ROM will not drive GPIO020 (DSW_PWROK) high in G3 sharing mode.

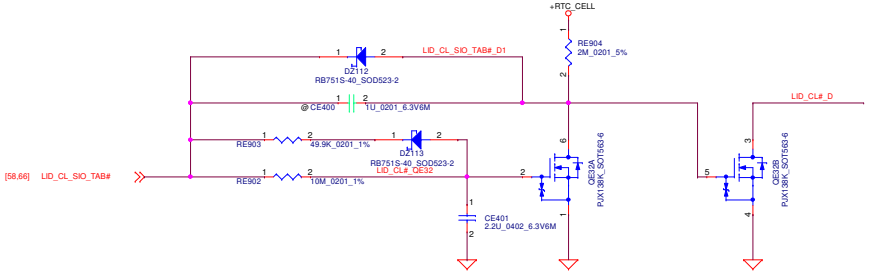
Boot Source Select (5200)
0=Use the Shared SPI pins for Boot
1=Use the eSPI Flash Channel for Boot

For Riverside UMA

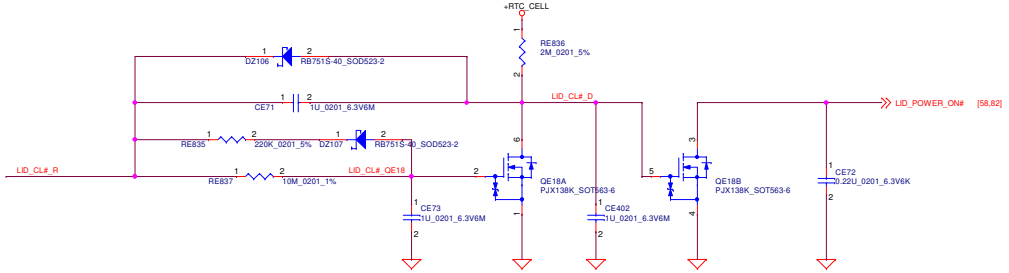


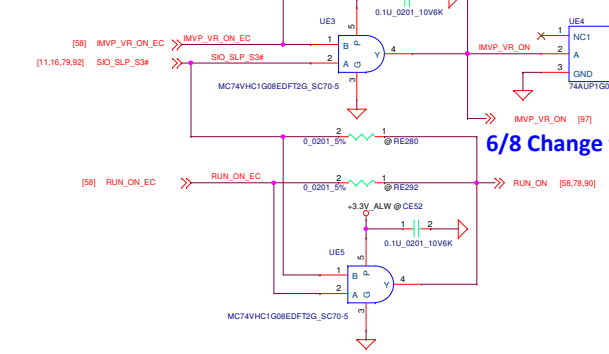


Fixed 360 auto power on

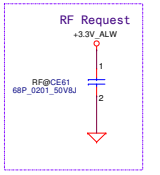


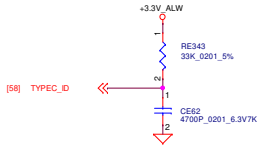
S5 LID OPEN POWER ON(Other Solution)





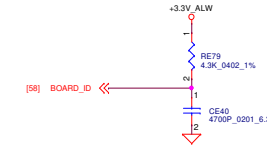
6/8 Change to SA00007WE00 DII





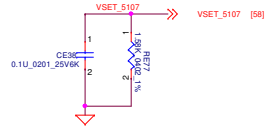
RE343	CE62	REV
240K	4700p	Single Port ACE w/o TR
130K	4700p	Single Port ACE w/TR
62K	4700p	Dual Port ACE w/o TR
* 33K	4700p	Dual Port ACE w/TR
8.2K	4700p	Dual Port ACE (w/TR +w/o TR)
4.3K	4700p	.
2K	4700p	
1K	4700p	

TYPEC_ID rise time is measured from 0%~63.2%.



RE79	CE40	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	X03
8.2K	4700p	reserved
* 4.3K	4700p	A00
2K	4700p	
1K	4700p	

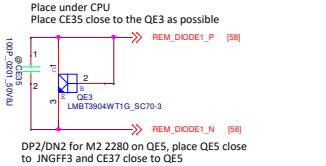
BOARD_ID rise time is measured from 0%~63.2%.



Rest=1.58K , Tp=96 degree
Rest=1.33K , Tp=93 degree

Thermal diode mapping

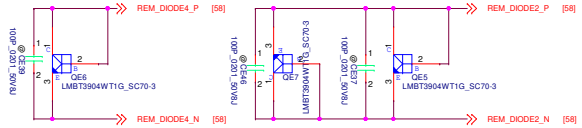
5107 Channel	Location
DP1/DN1	CPU (QE3)
DP2/DN2	Ambient (QE5)
DN2a/DP2a	DDR (QE7)
DP3/DN3	NA
DP4/DN4	CPU VR (QE6)

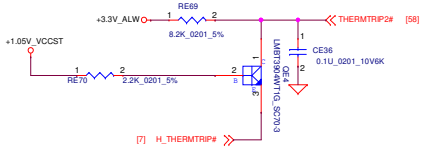


DP2/DN2 for M2 2280 on QE5, place QE5 close to JNGFF3 and CE37 close to QE5

DP4/DN4 for Skin on QE6, place QE6 close to Vcore VR choke.

DN2a/DP2a for DDR on QE7, place QE7 close to DDR and CE46 close to QE7





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Title: MEC5107 support

Size: Document Number: LA-K371P Rev: 1.0

Date: Wednesday, October 28, 2020 Sheet 59 of 125

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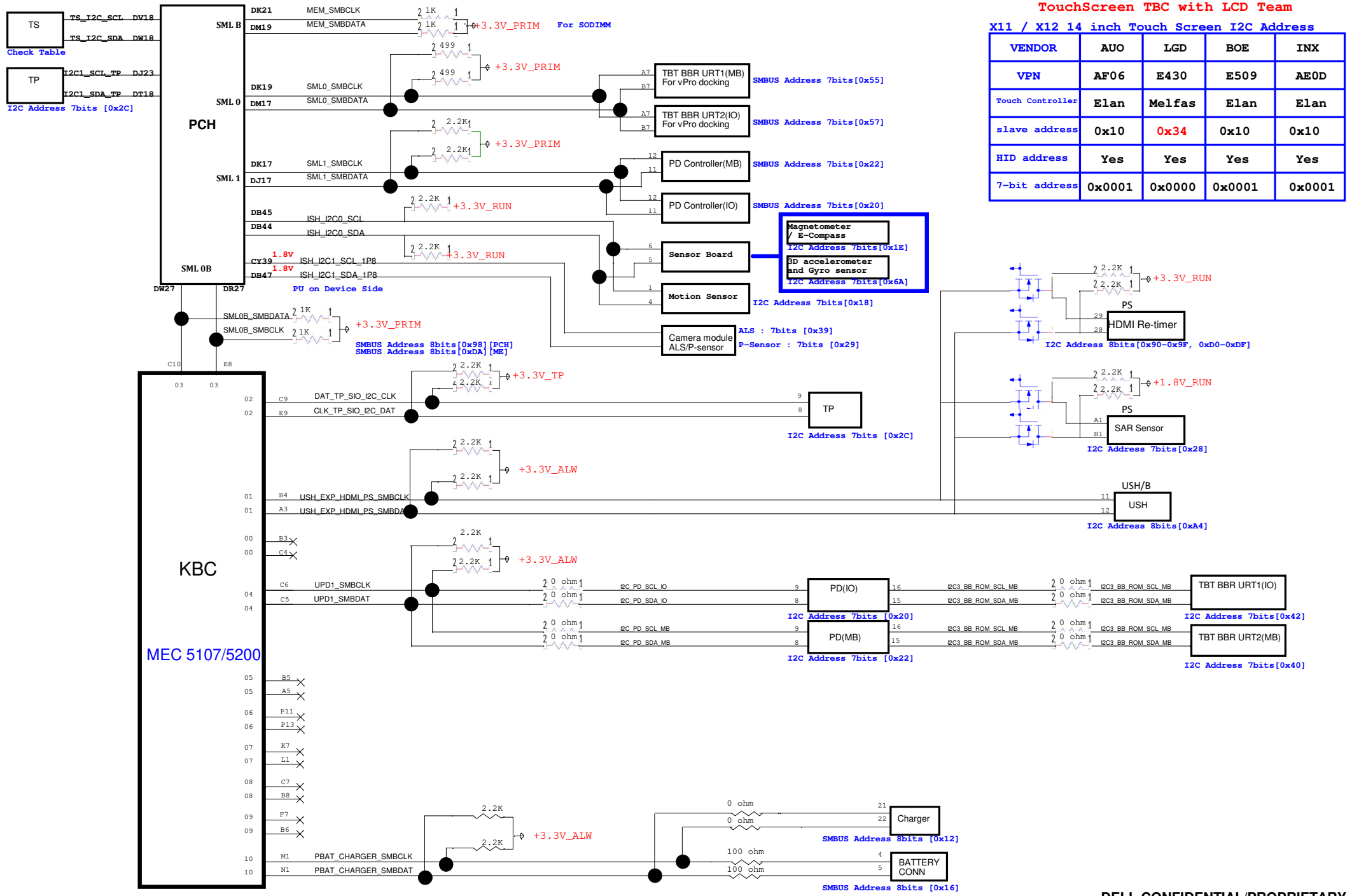
TouchScreen TBC with LCD Team
X11 / X12 14 inch Touch Screen I2C Address
VENDOR | AUO | LGD | BOE | INX
VPN | AF06 | E430 | E509 | AE0D
Touch Controller | Elan | Melfas | Elan | Elan
slave address | 0x10 | 0x34 | 0x10 | 0x10
HID address | Yes | Yes | Yes | Yes
7-bit address | 0x0001 | 0x0000 | 0x0001 | 0x0001
TS
TP
Check Table
I2C Address 7bits [0x2C]
PCH
SML B
SML 0
SML 1
SML 0B
MEM_SMBCLK
MEM_SMBDATA
For SODIMM
SML0_SMBCLK
SML0_SMBDATA
SML1_SMBCLK
SML1_SMBDATA
ISH_I2C0_SCL
ISH_I2C0_SDA
ISH_I2C1_SCL_1P8
ISH_I2C1_SDA_1P8
PU on Device Side
SML0B_SMBDATA
SML0B_SMBCLK
SMBUS Address 8bits[0x98] [PCH]
SMBUS Address 8bits[0xDA] [ME]
TBT BBR URT1(MB) For vPro docking
TBT BBR URT2(IO) For vPro docking
SMBUS Address 7bits[0x55]
SMBUS Address 7bits[0x57]
PD Controller(MB)
PD Controller(IO)
SMBUS Address 7bits[0x22]
SMBUS Address 7bits[0x20]
Sensor Board
Magnetometer / E-Compass
I2C Address 7bits[0x1E]
3D accelerometer and Gyro sensor
I2C Address 7bits[0x6A]
Motion Sensor
I2C Address 7bits[0x18]
Camera module ALS/P-sensor
ALS : 7bits [0x39]
P-Sensor : 7bits [0x29]
KBC
MEC 5107/5200
DAT_TP_SIO_I2C_CLK
CLK_TP_SIO_I2C_DAT
TP
I2C Address 7bits [0x2C]
USH_EXP_HDMI_PS_SMBCLK
USH_EXP_HDMI_PS_SMBDA
UPD1_SMBCLK
UPD1_SMBDAT
PD(IO)
I2C Address 7bits [0x20]
PD(MB)
I2C Address 7bits [0x22]
TBT BBR URT1(IO)
I2C Address 7bits[0x42]
TBT BBR URT2(MB)
I2C Address 7bits[0x40]
PBAT_CHARGER_SMBCLK
PBAT_CHARGER_SMBDAT
Charger
SMBUS Address 8bits [0x12]
BATTERY CONN
SMBUS Address 8bits [0x16]
PS
HDMI Re-timer
I2C Address 8bits[0x90-0x9F, 0xD0-0xDF]
SAR Sensor
I2C Address 7bits[0x28]
USH/B
USH
I2C Address 8bits[0xA4]
+3.3V_PRIM
+3.3V_RUN
+3.3V_TP
+3.3V_ALW
+1.8V_RUN
1.8V
DW27
DR27
C10
E8
DEL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
SMbus Block Diagram
LA-K371P
Rev 1.0
Wednesday, October 28, 2020
Sheet 61 of 125
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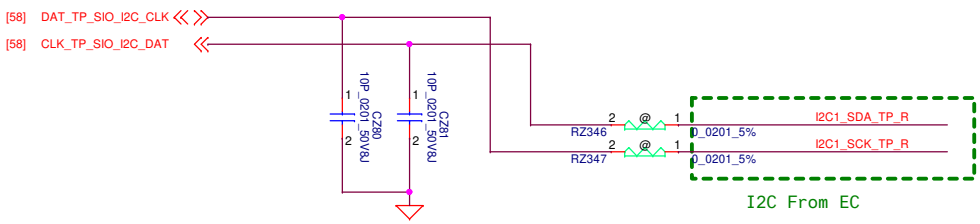
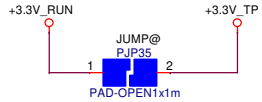
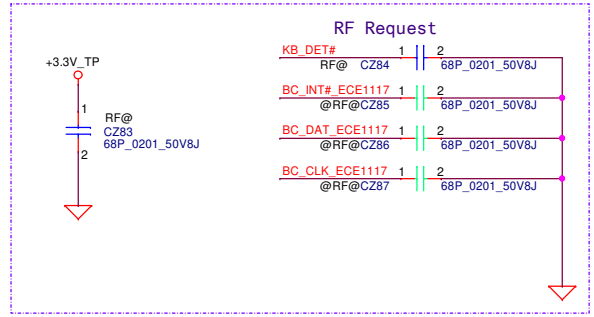
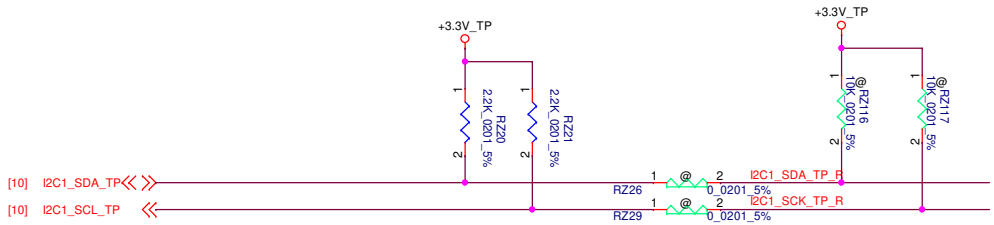
Touch Pad



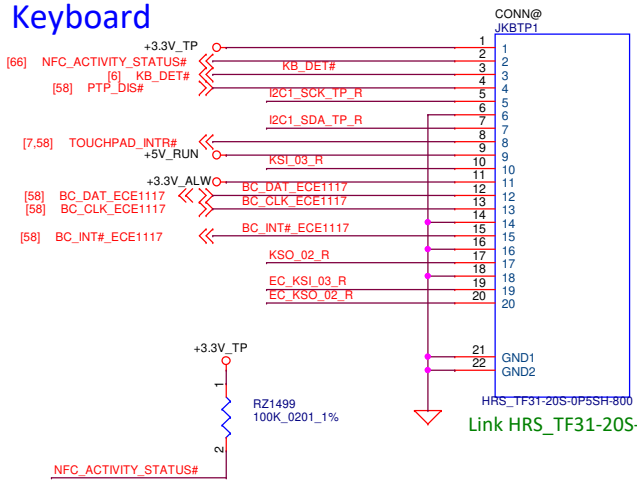


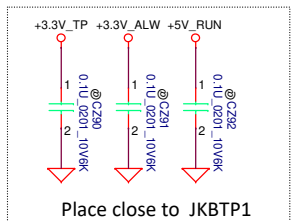




Plan is for I2C to be driven by the EC for Win7 and Pre-OS (will utilize Intel I2C drivers for Win7)
For Win8.1 and 10 the EC will control TP over I2C Pre-OS and then the PCH will drive I2C when in Windows
Route PS2 from EC to the touch pad also for contingency plan if I2C has issues

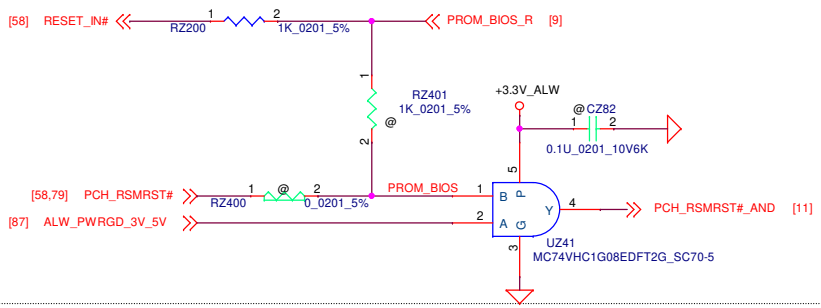
Keyboard



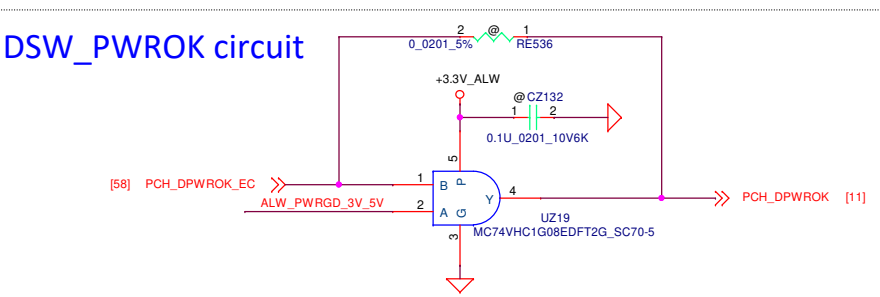


Link HRS_TF31-20S-0P5SH-800 done 0313

RSMRST circuit



DSW_PWROK circuit



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Title: Keyboard

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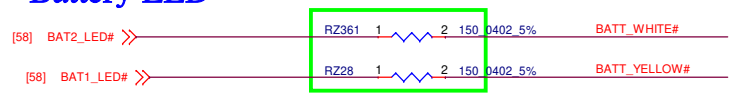
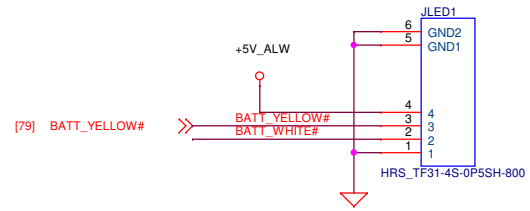
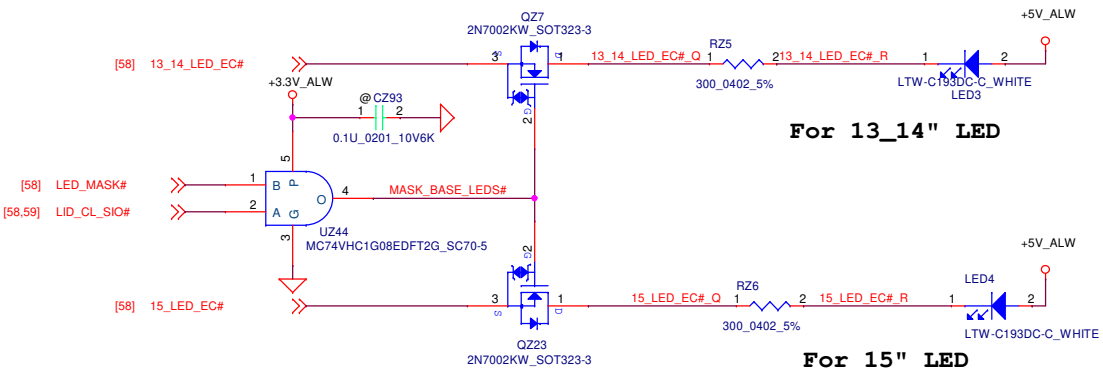
Battery LED



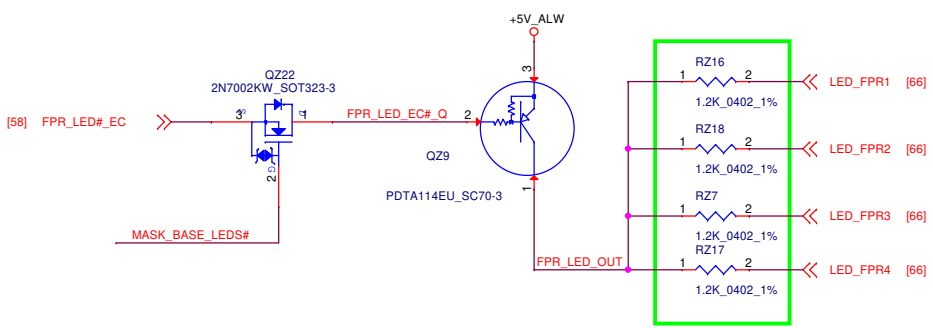
Could combine to Audio Board



Breath LED

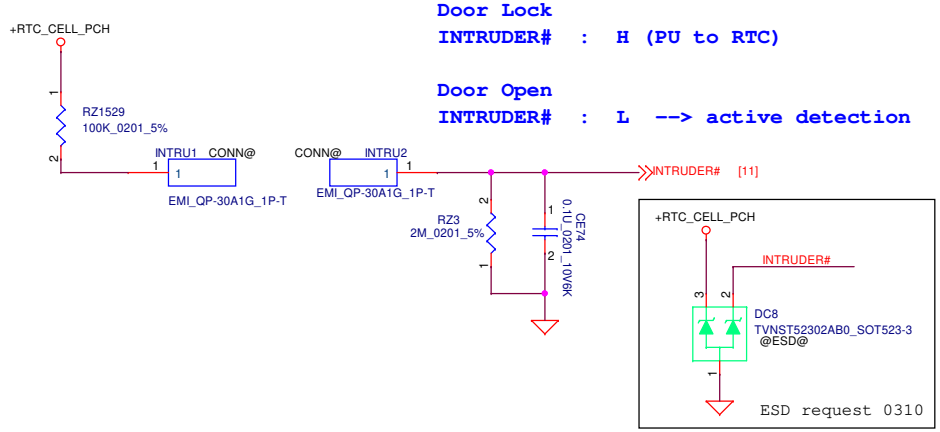


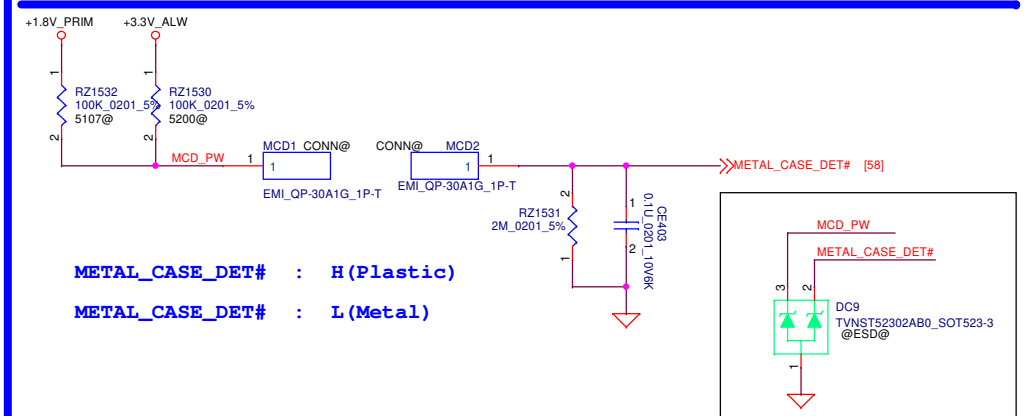
02/20 got the message update for LED * 4pcs inside FPR



Door Lock
INTRUDER# : H (PU to RTC)

Door Open
INTRUDER# : L --> active detection





METAL_CASE_DET# : H(Plastic)

METAL_CASE_DET# : L(Metal)

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Title: LED & LID		
Size	Document Number: LA-K371P	Rev: 1.0
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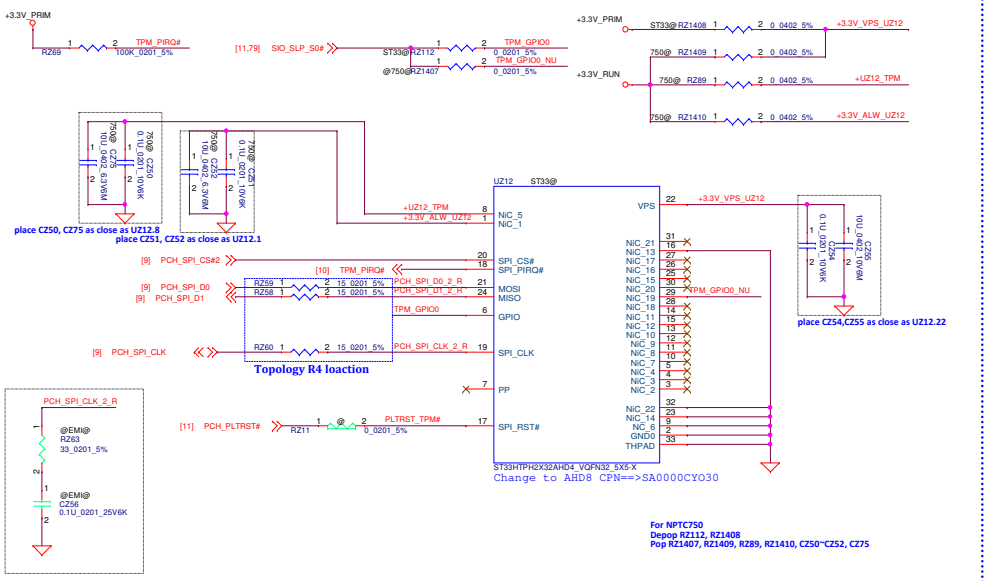
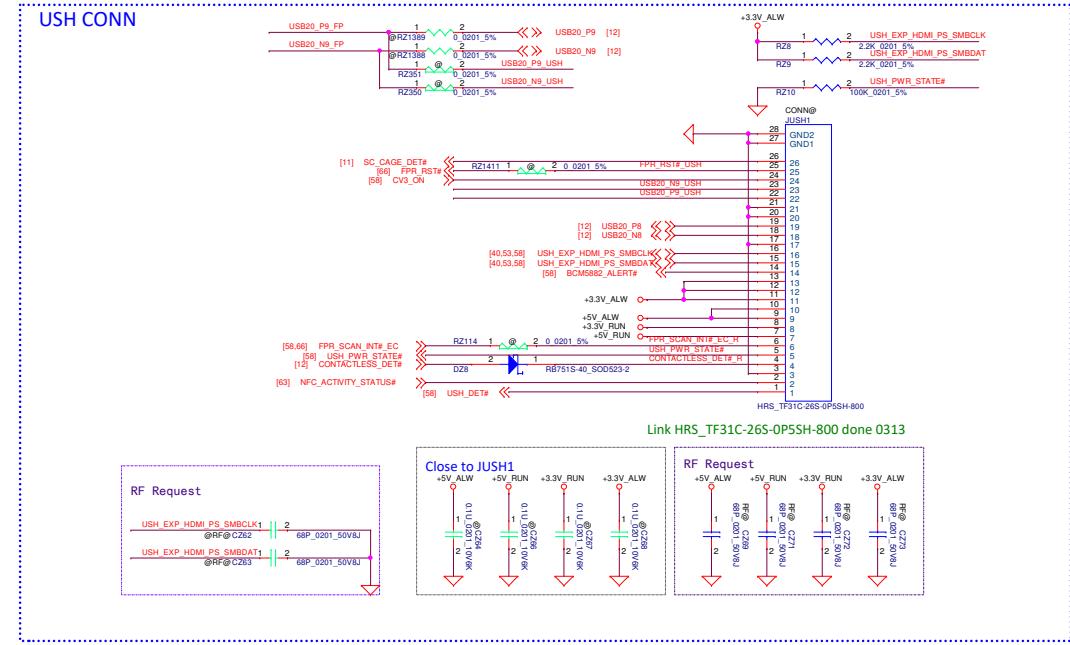
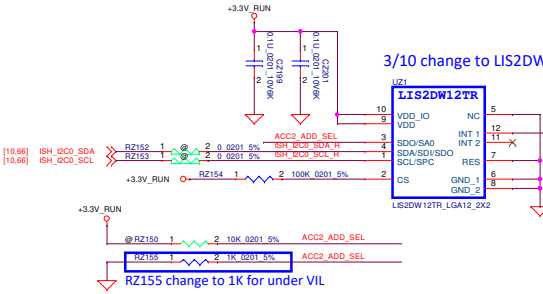
For ST/Nuvoton TPM



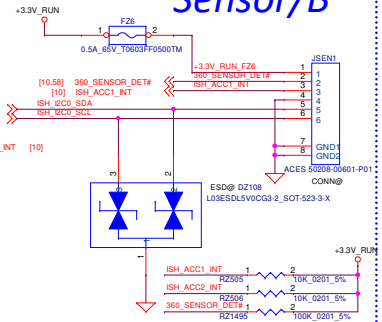
USH CONN



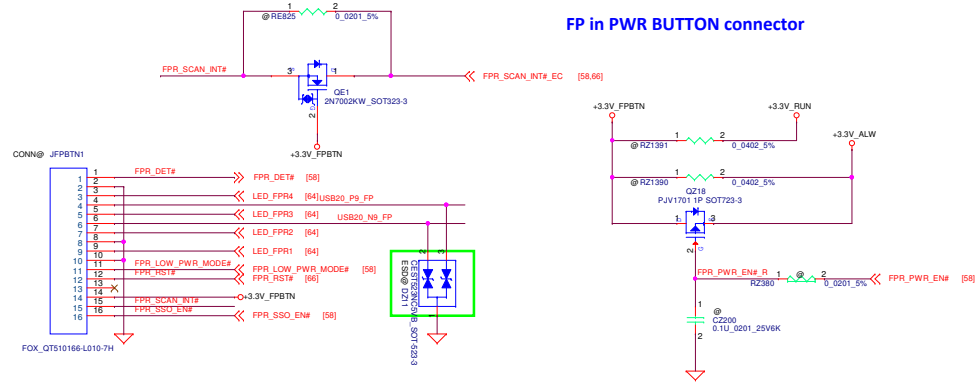
Accelerometer



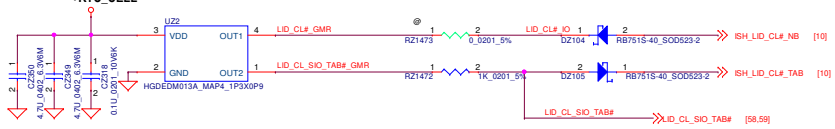
Sensor/B



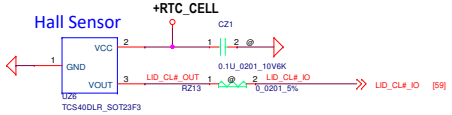
FP in PWR BUTTON connector



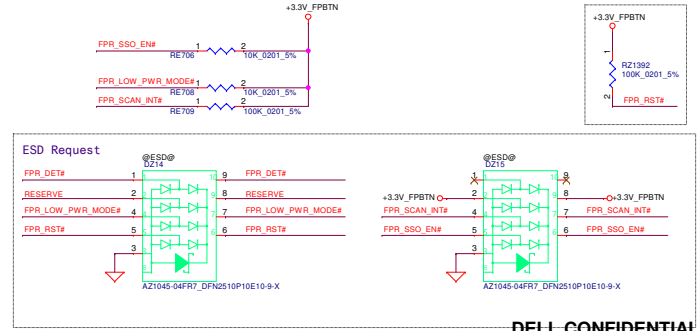
GMR Sensor



Hall Sensor



Compal MB CONN Symbol	Signal	FPR Symbol
2	GND	1
4	USB DP(D+)	2
6	USB DM(D-)	3
8	GND	4
10	GND	5
12	FP RESET#	6
14	+3.3V_FPBTN	7
16	FPR_SSO_EN#	8
15	FPR_SCAN_INT#	9
13	NC	10
11	FPR_LOW_PWR_MODE#	11
9	FPR_LED_1	12
7	FPR_LED_2	13
5	FPR_LED_3	14
3	FPR_LED_4	15
1	FPR DET(GND)	16



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Title: USH & TPM

Size: Document Number: LA-K371P

Rev: 1.0

Date: Wednesday, October 28, 2020

Sheet: 66 of 125

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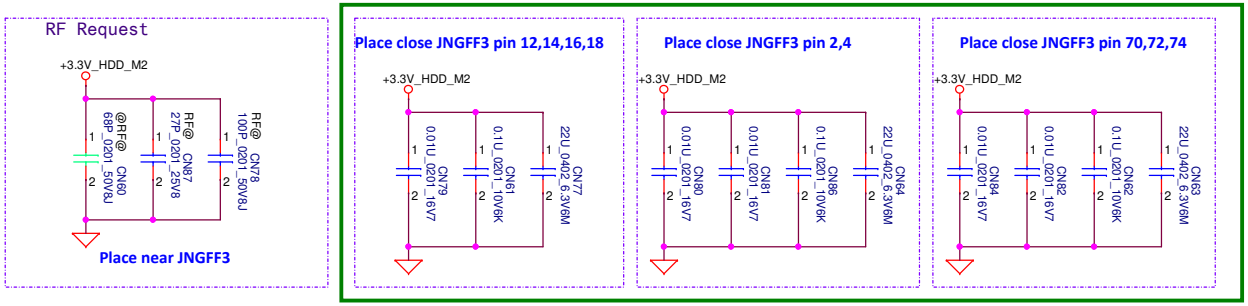
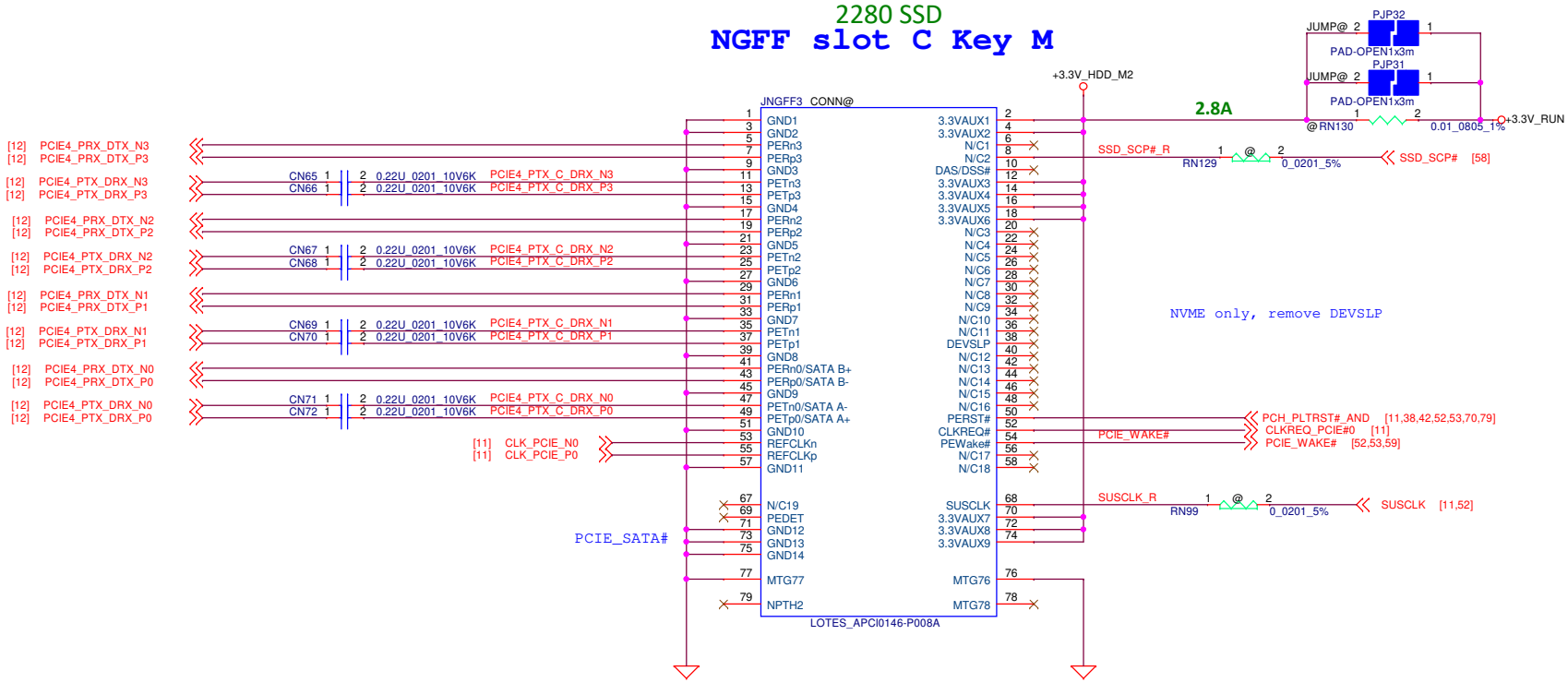
Add Power Decoupling for support Intel Teton Glacier



2280 SSD

NGFF slot C Key M



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Title: M2 2280 Socket

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Date: Wednesday, October 28, 2020 | Sheet 68 of 125

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For PCIE Interface

uSD Sub Board Keeping in Main Board

+3.3V_RUN — JUMP@ PJP14 — +3.3V_MMI_IN

PAD-OPEN1x2m

+3.3V_MMI_IN — RR20 2 @ 1 0_0402_5% — +3.3V_MMI_AUX

+3.3V_MMI_AUX — RR19 2 1 10K_0201_5% — MEDIACARD_IRQ#

uSD Sub Board Keeping in Main Board

+3.3V_MMI_AUX: CR1 4.7U_0402_6.3V6M; CR2 0.1U_0201_10V6K

+3.3V_MMI_IN: CR3 0.1U_0201_10V6K; CR4 10U_0402_6.3V6M

UR1 RTS5242 RTS5242-GR_QFN32_4X4-X

[11,38,42,52,53,68,79]	PCH_PLTRST#_AND	PERST#
[11]	CLKREQ_PCIE#4	CLK_REQ#
[11]	CLK_PCIE_P4	REFCLKP
[11]	CLK_PCIE_N4	REFCLKN
[12]	PCIE_PTX_DRX_P7	HSIP
[12]	PCIE_PTX_DRX_N7	HSIN
[12]	PCIE_PRX_DTX_P7	HSOP
[12]	PCIE_PRX_DTX_N7	HSON
[9]	MEDIACARD_IRQ#	WAKE#
SD/MMCCD#		MS_INS#
		SD_CD#

3V3aux 3V3_IN (27, 11)

CARD_3V3 DV33_18 (12, 18) — +3.3V_RUN_CARD — CR22 1U_0201_6.3V6M

SP1 SD/MMCDAT1/RCLK-
SP2 SD/MMCDAT0/RCLK+
SP3 SD/MMCCLK
SP4 SD/MMCCMD @EMI@
SP5 SD/MMCDAT3
SP6 SD/MMCDAT2
SP7 SDWP

RR9 RR10 RR5 RR6 RR7 RR8: @ 0_0201_5%

SD/MMCDAT1/RCLK-_R; SD/MMCDAT0/RCLK+_R; SD/MMCCLK_R; SD/MMCCMD_R; SD/MMCDAT3_R; SD/MMCDAT2_R

@EMI@ CR21 5P_0402_50V8C — EMI depop location

+1.2V_LDO: CR5 4.7U_0402_10V6M; CR6 0.1U_0201_10V6K; CR7 0.1U_0201_10V6K

AV12 DV12S (10, 14)

+1.8V_RUN_CARD — SD_VDD2 (13)

+RREF — RREF (9) — RR4 6.2K_0402_1%

7/18 Vender suggest

SD_LN1_P SD_LN1_M: SD_UHS2_D1P, SD_UHS2_D1N (22, 23)

SD_LN0_P SD_LN0_M: SD_UHS2_D0P, SD_UHS2_D0N (26, 25)

SDREG2 GPIO (24, 28): +SDREG2_CR15 1U_0201_6.3V6M; SD_GPIO_2 — 10K_0201_5% — RR3 — +3.3V_MMI_AUX

E-PAD (33)

RF Request

+3.3V_MMI_AUX: @RF@ CR27 12P_0201_50V8J; @RF@ CR28 82P_0201_50V8J

+3.3V_MMI_IN: @RF@ CR25 12P_0201_50V8J; @RF@ CR26 82P_0201_50V8J

QR1 2N7002KW_SOT323-3

SDWP — [10] HOST_SD_WP#

uSD Sub Board Keeping in Main Board

+3.3V_RUN_CARD: CR17 0.1U_0201_10V6K; CR18 4.7U_0402_10V6M — CR17,CR18 near JSD1.4

+1.8V_RUN_CARD: CR19 0.1U_0201_10V6K; CR20 4.7U_0402_10V6M — CR19,CR20 near JSD1.14

JSD1 CONN@ T-SOL_158-1240902600

+3.3V_RUN_CARD, +1.8V_RUN_CARD

SD/MMCCMD_R	CMD
SD/MMCCLK_R	CLK
SD/MMCCD#	CD
	SWIO
SD/MMCDAT0/RCLK+_R	DAT0/RCLK+
SD/MMCDAT1/RCLK-_R	DAT1/RCLK-
SD/MMCDAT2_R	DAT2
SD/MMCDAT3_R	CD/DAT3
SD_UHS2_D0P	D0+
SD_UHS2_D0N	D0-
SD_UHS2_D1P	D1+
SD_UHS2_D1N	D1-

VDD1 (4, 15), VDD2 (3), VSS1 (6, 17), VSS2 (20), VSS3 (23), VSS4 (24), NPTH1, GND1 (10, 11), GND2 (12), GND3 (13), GND4 (14), GND5 (25), NPTH2

HOST_SD_WP#	SDWP	STATUS
High	Low	Write Enable
Low	High	Write Protect(FW LOCK)

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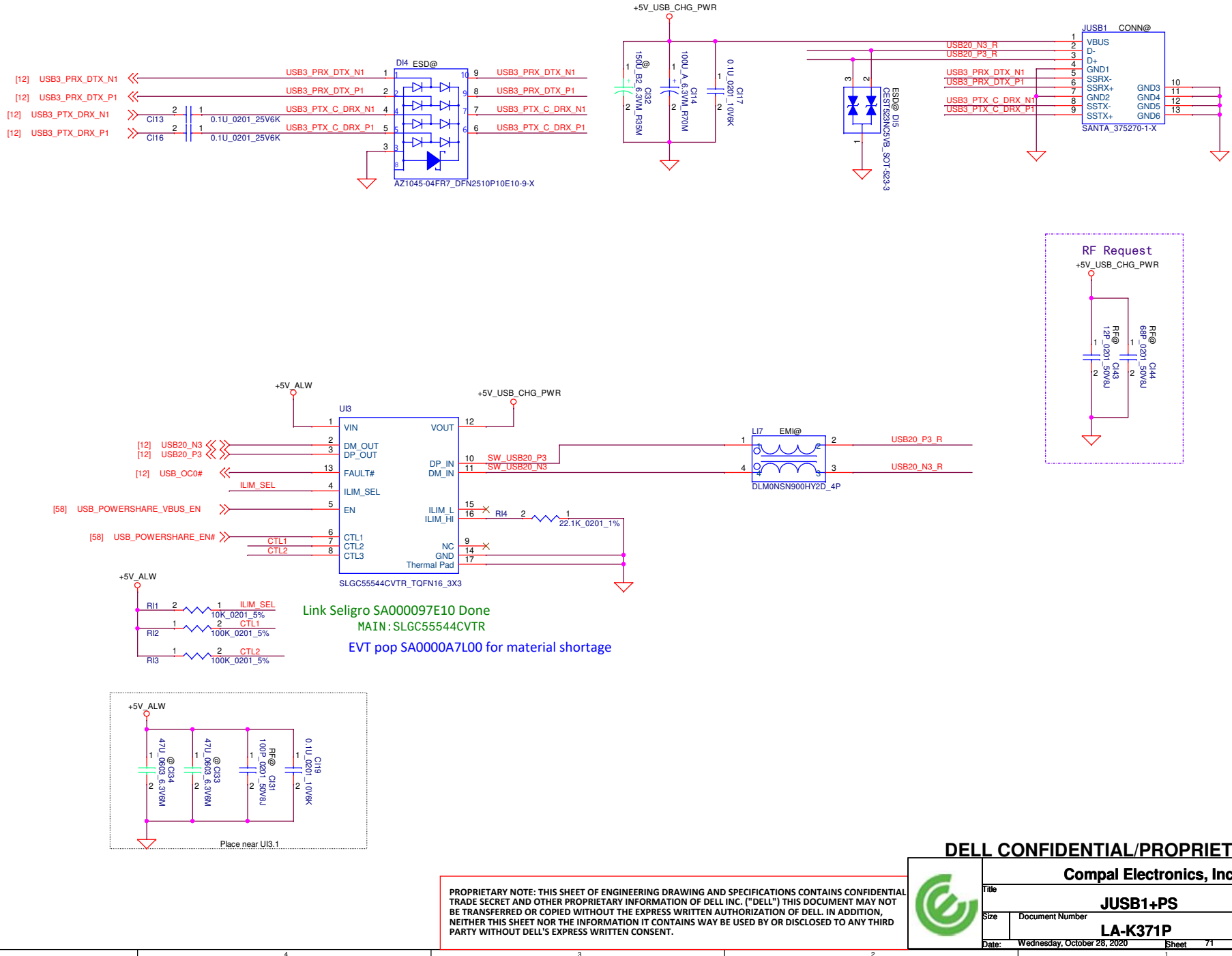
Compal Electronics, Inc.

Title: Card Reader RTS5242

Size | Document Number: LA-K371P | Rev: 1.0

Date: Wednesday, October 28, 2020 | Sheet 70 of 125



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Compal Electronics, Inc.

Title	JUSB1+PS	
Size	Document Number: LA-K371P	Rev: 1.0
Date: Wednesday, October 28, 2020	Sheet 71 of 125	

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+3.3V_RUN

RE48 1 2 PWM_FAN1 10K_0201_5%

RE51 1 2 TACH_FAN1 10K_0201_5%

Link 50271-0040N-001 done 0123

CONN@ JFAN1 GND2 GND1 6 5 4 3 2 1

CVILU_CI1104M2HR1-NH

PWM_FAN1 TACH_FAN1

PWM_FAN1 [58] TACH_FAN1 [58] +5V_RUN

10U_0402_6.3V6M CE32

@ DE1 BZV55-B5V6_SOD80C2

Fan

POWER & INSTANT ON SWITCH TOP

[59,79] POWER_SW#_MB POWER_SW#_MB SW5 SKRBACE010_4P-X

FOR 13/14 PWR BUTTON

POWER & INSTANT ON SWITCH TOP

POWER_SW#_MB SW6 SKRBACE010_4P-X

FOR 15 PWR BUTTON

PWR Choke

CLIP5_CONN@ P1 EMIST_SUL-12A2M_1P

CLIP6_CONN@ P1 EMIST_SUL-12A2M_1P

CLIP7_CONN@ P1 EMIST_SUL-12A2M_1P

JUSB CLIPS

CLIP34CONN@ P1 CLIP_0P8X4P4

CLIP35CONN@ P1 CLIP_0P8X10P0

CLIP33CONN@ P1 CLIP_0P8X4P4

CLIP36CONN@ P1 CLIP_0P8X4P4

CLIP37CONN@ P1 CLIP_0P8X10P0

CLIP38CONN@ P1 CLIP_0P8X5P3

WWAN

CLIP1_CONN@ P1 EMIST_SUL-12A2M_1P

CLIP2_CONN@ P1 EMIST_SUL-12A2M_1P

CLIP3_CONN@ P1 EMIST_SUL-12A2M_1P

CLIP4_CONN@ P1 EMIST_SUL-12A2M_1P

BOT CLIPS

CLIP11CONN@ P1 EMIST_SUL-15A3M

CLIP13CONN@ P1 EMIST_SUL-15A3M

CLIP17CONN@ P1 EMIST_SUL-15A3M

CLIP18CONN@ P1 EMIST_SUL-15A3M

CLIP12CONN@ P1 EMIST_SUL-15A3M

CLIP15CONN@ P1 EMIST_SUL-15A3M

CLIP9_CONN@ P1 EMIST_SUL-25M

CLIP14CONN@ P1 EMIST_SUL-25M

CLIP10CONN@ P1 EMIST_SUL-25M

CLIP16CONN@ P1 EMIST_SUL-25M

CLIP19CONN@ P1 EMIST_SUL-25M

CLIP22CONN@ P1 EMIST_SUL-25M

CLIP39CONN@ P1 EMIST_SUL-25M

CLIP27CONN@ P1 EMIST_SUL-25M

CLIP28CONN@ P1 EMIST_SUL-25M

Fiducial Mark

@FD1 FIDUCIAL MARK~D

@FD2 FIDUCIAL MARK~D

@FD3 FIDUCIAL MARK~D

@FD4 FIDUCIAL MARK~D

CPU

@H1 H_3P7 @H2 H_3P7 @H3 H_3P7 @H4 H_3P7 @H5 H_3P5 @H6 H_3P5 @H7 H_3P8 @H8 H_2P5 @H9 H_2P5 @H10 H_3P5 @H12 H_3P5 @H18 H_3P6

@H15 H_2P6X2P3 @H16 H_3P5X1P0N @H17 H_3P5X1P0N @H13 H_3P2 @H14 H_3P2

DDR Clip Remove all 2020/2/25

Gasket

CLIP31CONN@ P1 RND-2P0X1P5x15

CLIP32CONN@ P1 RND-2P0X1P5x18

SHDCAN CONN@ P1 SION_C7521R_1P-T

TBT Crystal

EDP

@ST1 CLIP_C6P5-D3PM @ST2 CLIP_C6P5-D3PM

SSD

@ST3 CLIP_C6P5-D3PM @ST4 CLIP_C6P5-D3PM

WLAN

@ST5 CLIP_C6P5-D3PM

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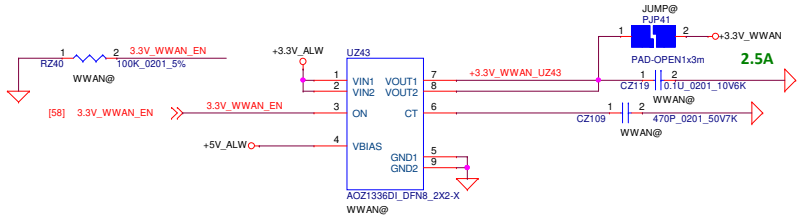
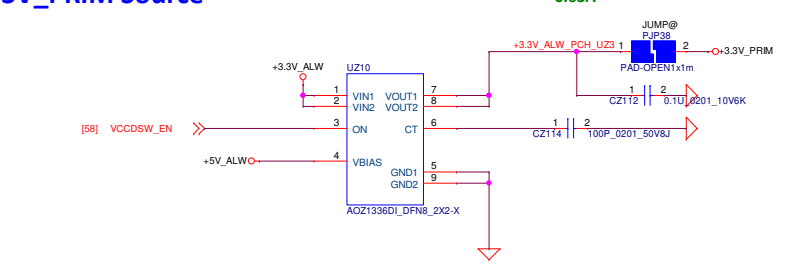
Title: PWRBTN, PAD, ME, FAN		
Size	Document Number: LA-K371P	Rev: 1.0
Date: Wednesday, October 28, 2020	Sheet 77 of 125	

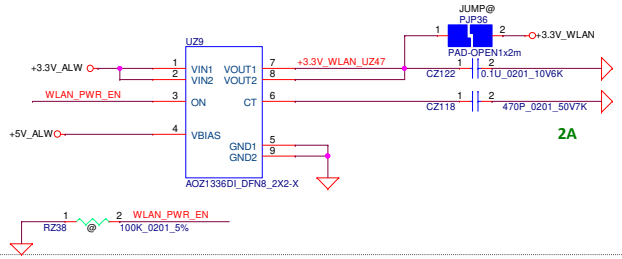
+3.3V_WWAN source



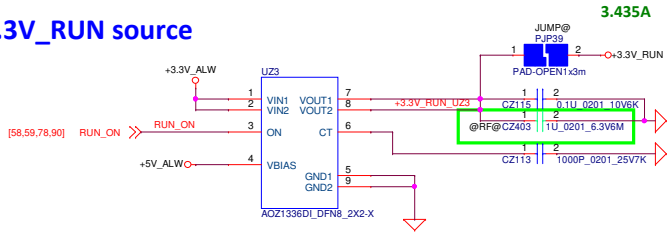
+3.3V_PRIM Source



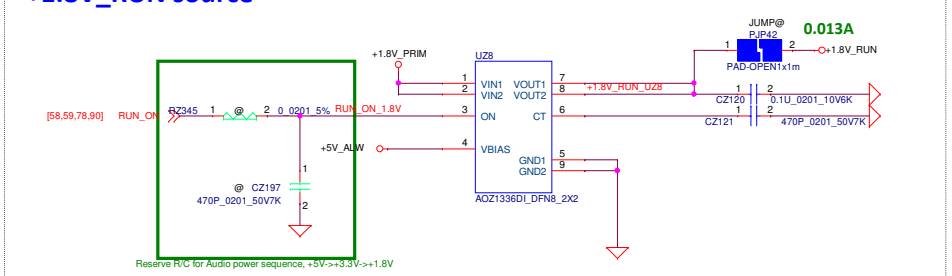
+3.3V_WLAN source



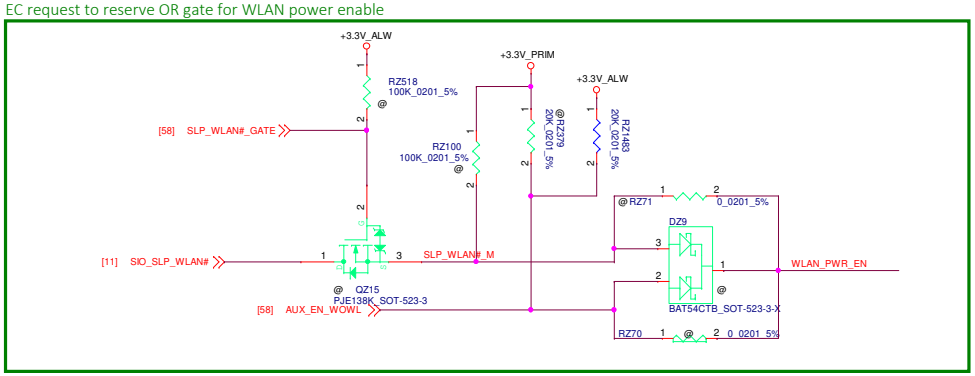
+3.3V_RUN source



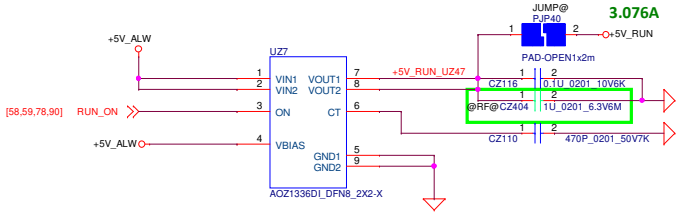
+1.8V_RUN source



EC request to reserve OR gate for WLAN power enable

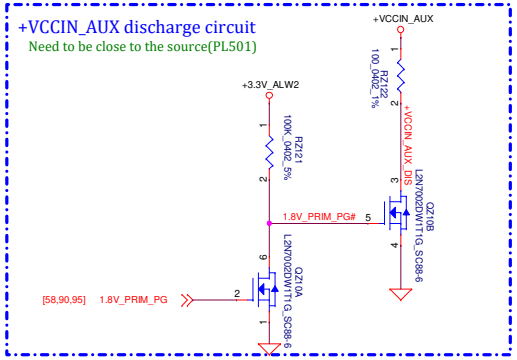


+5V_RUN source



+VCCIN_AUX discharge circuit

Need to be close to the source(PL501)



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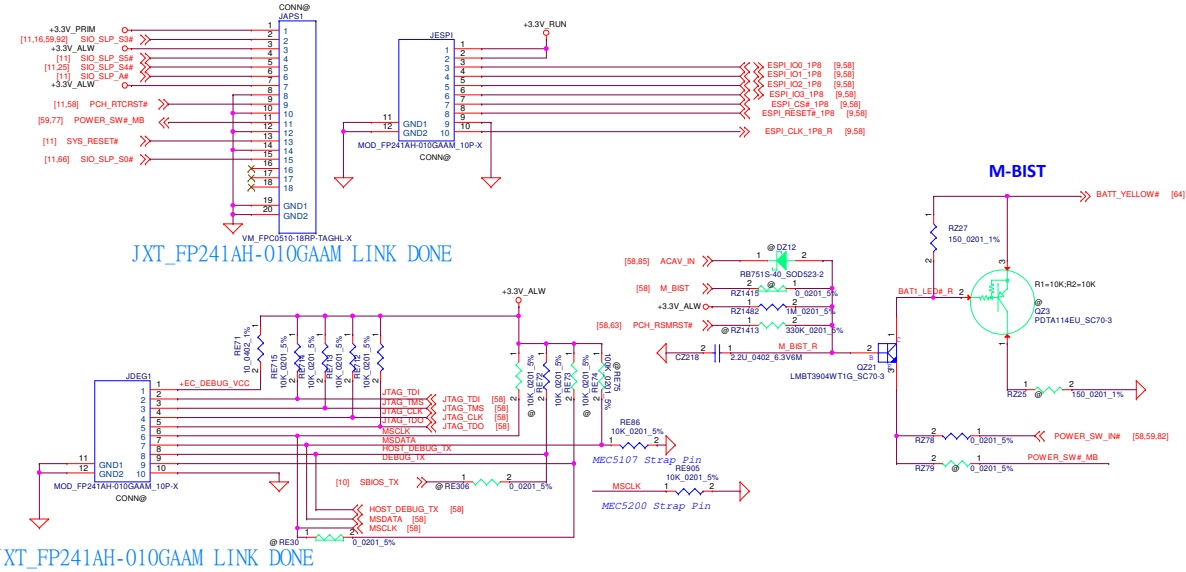
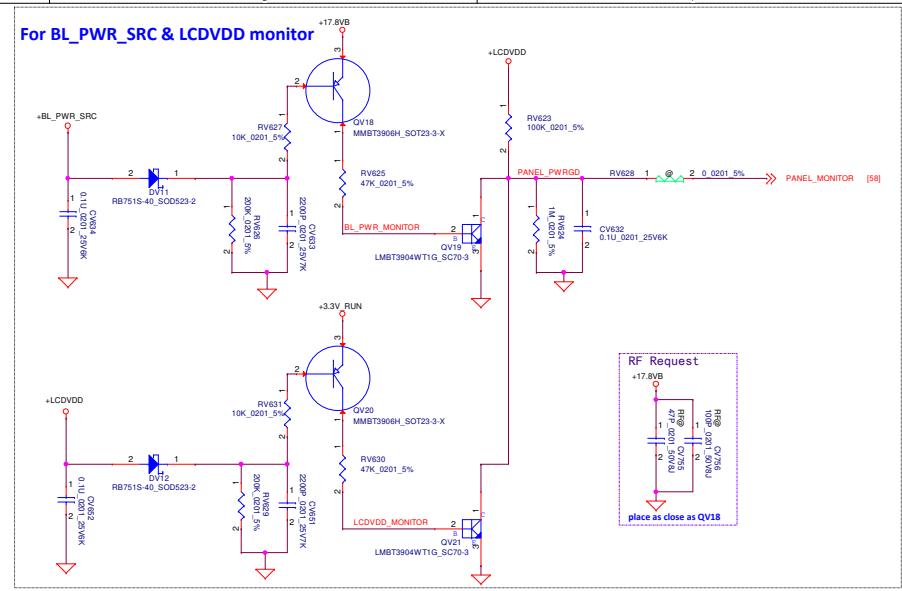
Compal Electronics, Inc.

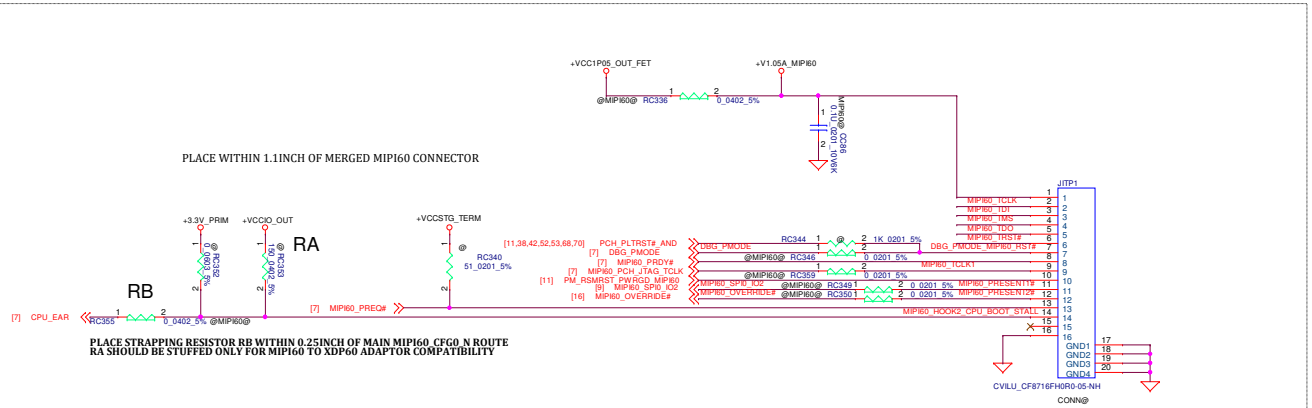
Title: Power control

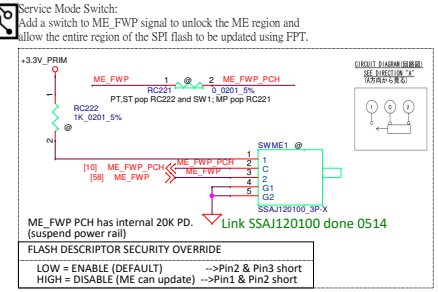
Size | Document Number: LA-K371P | Rev: 1.0

Date: Wednesday, October 28, 2020 | Sheet 78 of 125









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Compal Electronics, Inc.

Title: XDP/CMC/APS...debug

Size: | Document Number: LA-K371P | Rev: 1.0

Date: Wednesday, October 28, 2020 | Sheet 79 of 125

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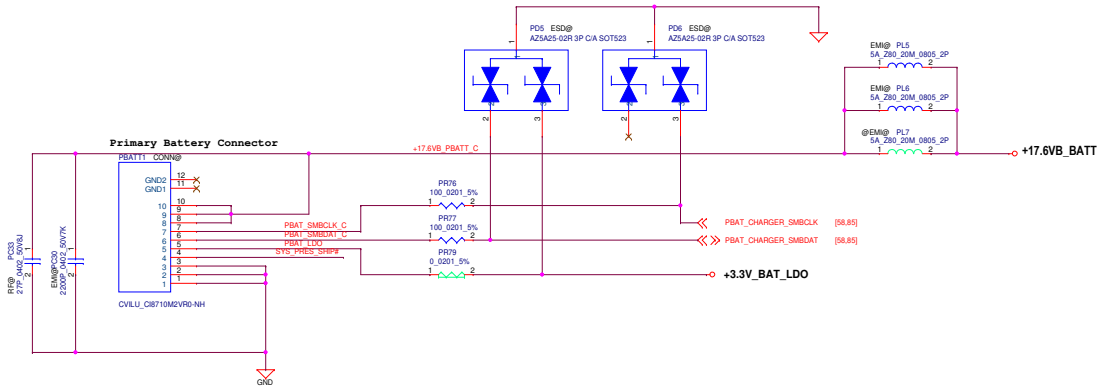
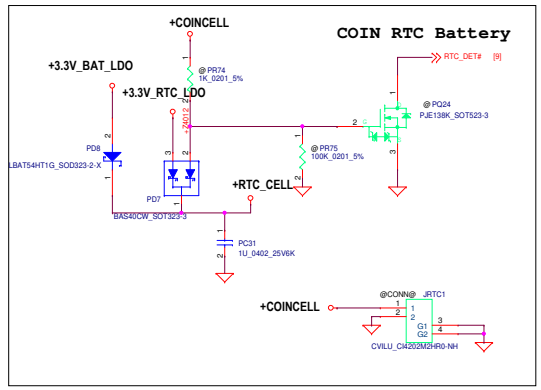
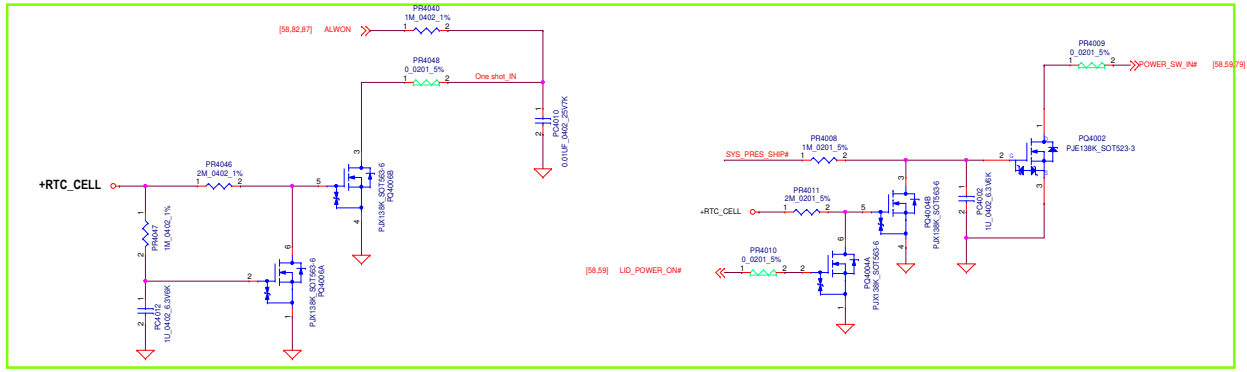
Compal Electronics, Inc.		
Title: PWR-Block Diagram		
Size	Document Number: LA-K371P	Rev: 1.0
Date: Wednesday, October 28, 2020	Sheet 81 of 125	

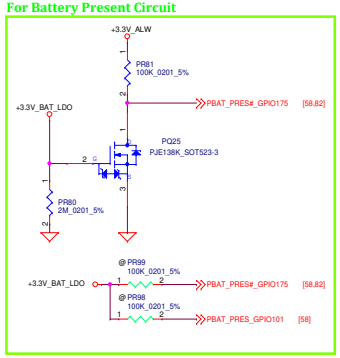






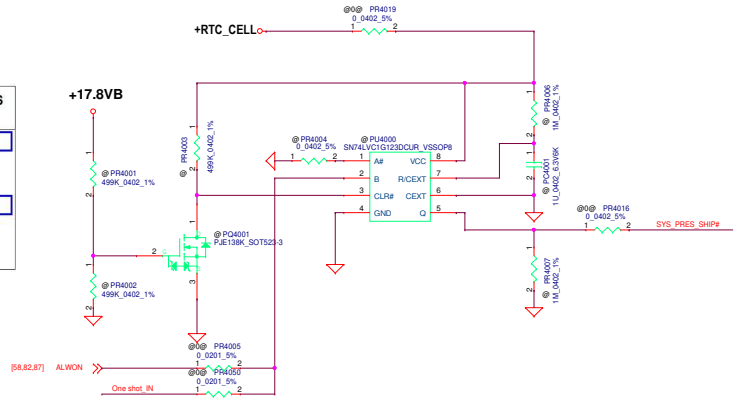
Storage mode wake up circuit

For Battery Present Circuit

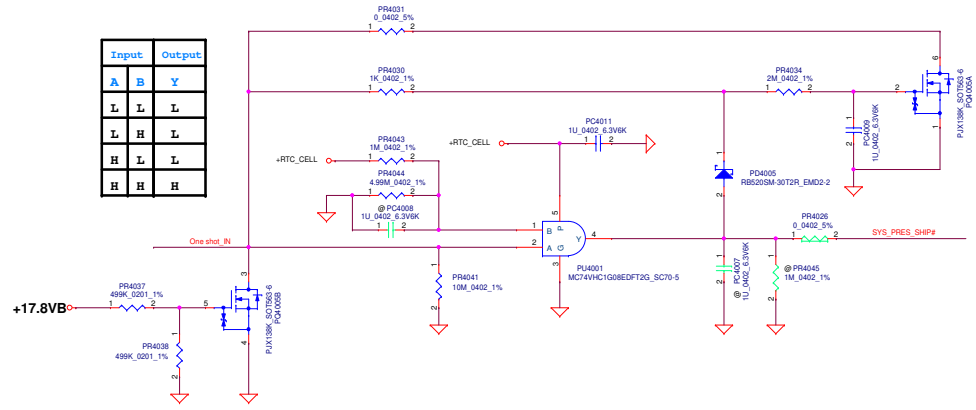


FUNCTION TABLE

INPUTS			OUTPUTS
$\overline{CLR}$	$\overline{A}$	B	Q
L	X	X	L
X	H	X	L(1)
X	X	L	L(1)
H	L	↑	⎍
H	↓	H	⎍
↑	L	H	⎍



Input		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H



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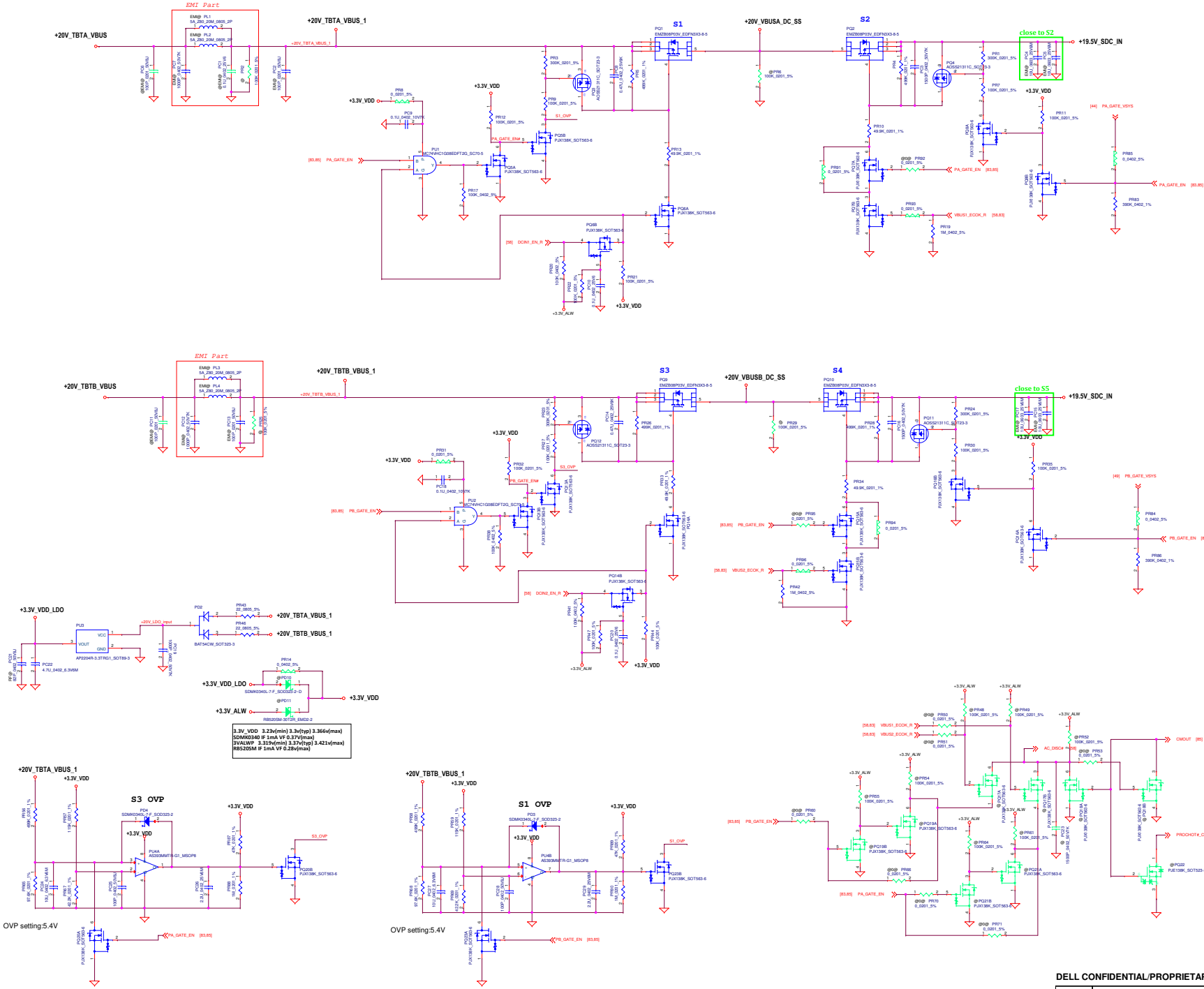
Compal Electronics, Inc.

Title: Battery Connector/ RTC

Size: Document Number: LA-K371P Rev: 1.0

Date: Wednesday, October 28, 2020 Sheet 82 of 125


EMI Part
+20V_TBTA_VBUS
+20V_TBTA_VBUS_1
S1
+20V_VBUSA_DC_SS
S2
close to S2
+19.5V_SDC_IN
+3.3V_VDD
PA_GATE_EN
PA_GATE_VSYS
VBUS1_ECOK_R
DCIN1_EN_R
+3.3V_ALW
EMI Part
+20V_TBTB_VBUS
+20V_TBTB_VBUS_1
S3
+20V_VBUSB_DC_SS
S4
close to S5
+19.5V_SDC_IN
PB_GATE_EN
PB_GATE_VSYS
VBUS2_ECOK_R
DCIN2_EN_R
+3.3V_VDD_LDO
+20V_LDO_input
AP2204R-3.3TR-G1_SOT89-3
BAT54CW_SOT323-3
SDMK0340L-7-F_SOD323-2-D
RB520SM-30T2R_EMD2-2
3.3V_VDD 3.23v(min) 3.3v(typ) 3.366v(max)
SDMK0340 IF 1mA VF 0.37V(max)
3VALWP 3.319v(min) 3.37v(typ) 3.421v(max)
RB520SM IF 1mA VF 0.28v(max)
S3 OVP
OVP setting:5.4V
S1 OVP
OVP setting:5.4V
CMOUT
PROCHOT#_CHG
AC_DET#
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
2TypeC PD Selector
LA-K371P
Wednesday, October 28, 2020

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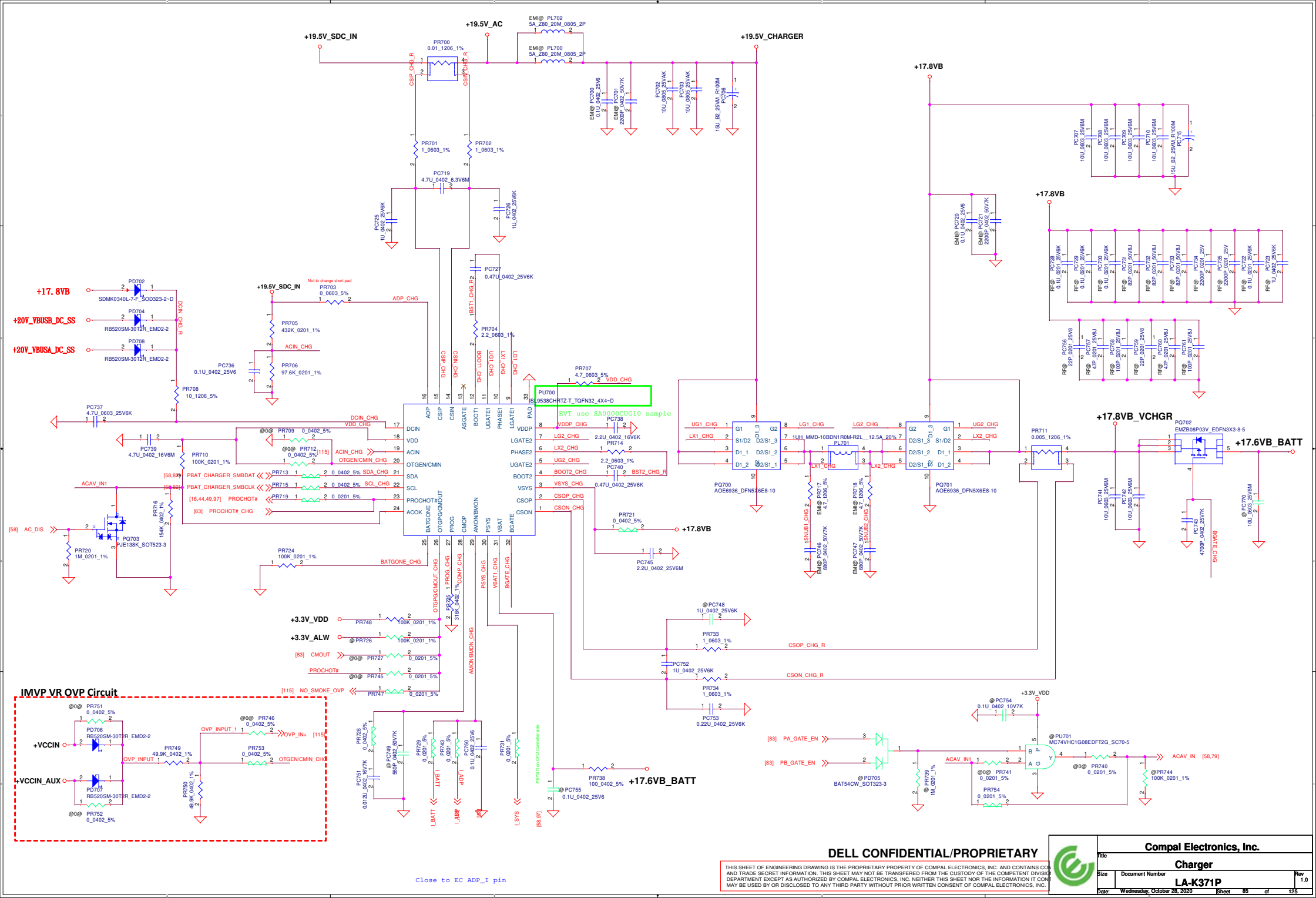
+19.5V_SDC_IN
+19.5V_AC
+19.5V_CHARGER
+17.8VB
+17.8VB_VCHGR
+17.6VB_BATT
+17. 8VB
+20V_VBUSB_DC_SS
+20V_VBUSA_DC_SS
+3.3V_VDD
+3.3V_ALW
IMVP VR OVP Circuit
+VCCIN
+VCCIN_AUX
PU700
SL9538CHRTZ-T_TQFN32_4X4-D
EVT use SA0000CUG10 sample
PQ700
AOE6936_DFN5X6E8-10
PQ701
AOE6936_DFN5X6E8-10
PQ702
EMZB08P03V_EDFN3X3-8-5
PQ703
PJE138K_SOT523-3
PD702
SDMK0340L-7-F_SOD323-2~D
PD704
RB520SM-30T2R_EMD2-2
PD708
RB520SM-30T2R_EMD2-2
PD706
RB520SM-30T2R_EMD2-2
PD707
RB520SM-30T2R_EMD2-2
PD705
BAT54CW_SOT323-3
PU701
MC74VHC1G08EDFT2G_SC70-5
PL701
1UH_MMD-10BDN1R0M-R2L_12.5A_20%
Close to EC ADP_I pin
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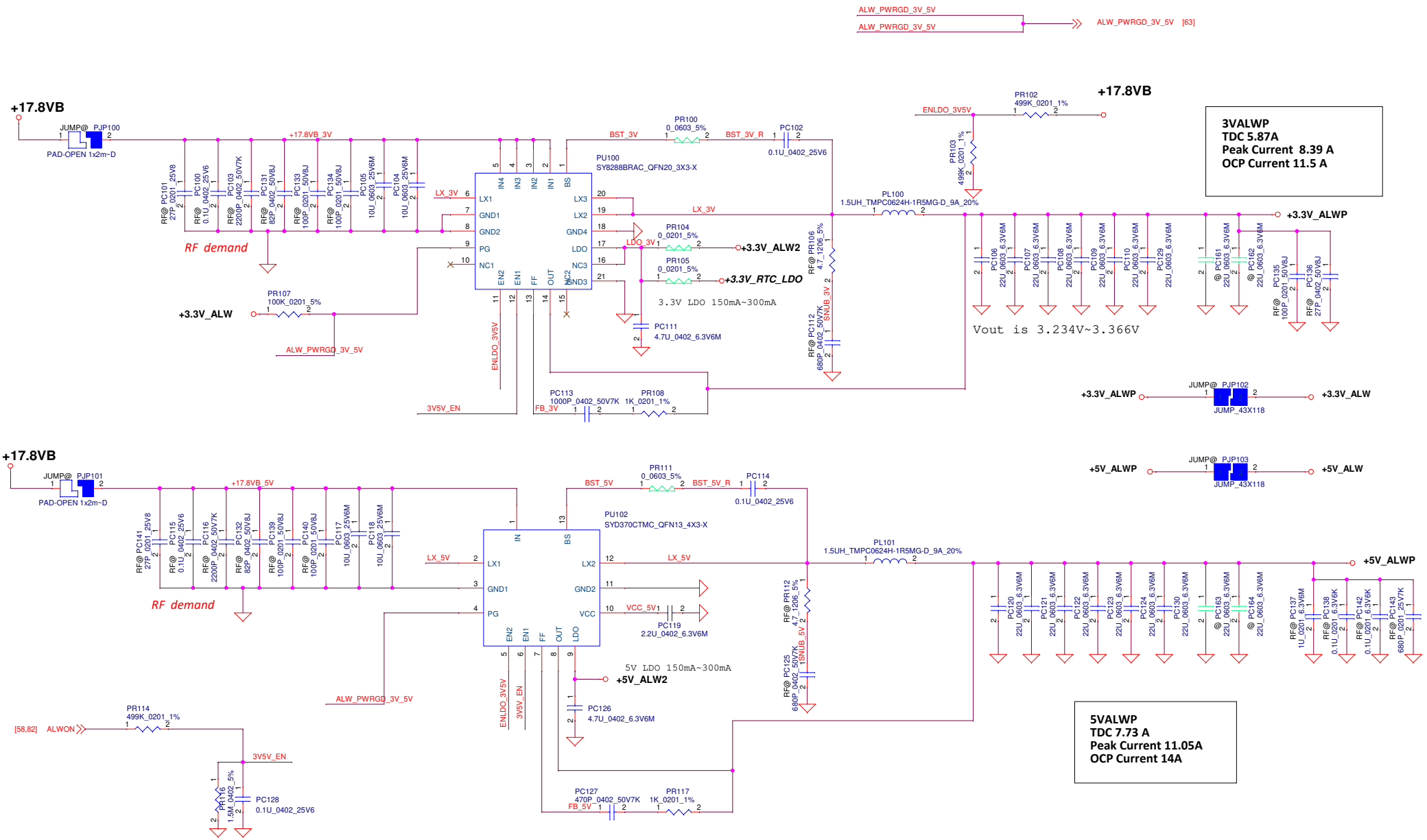

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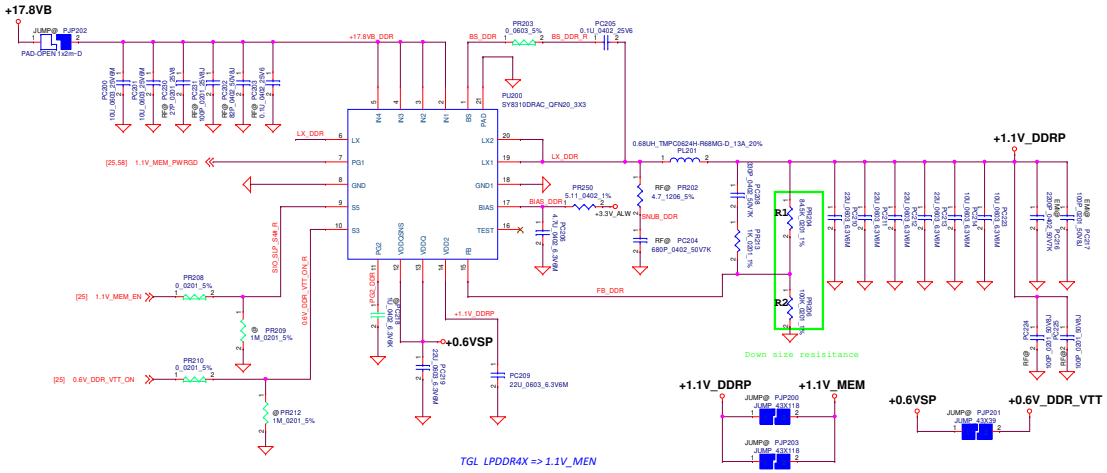

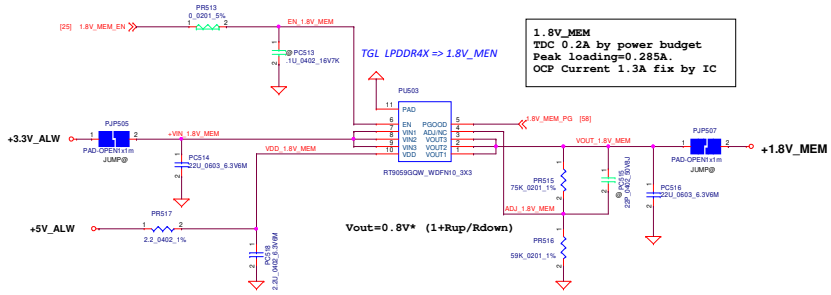

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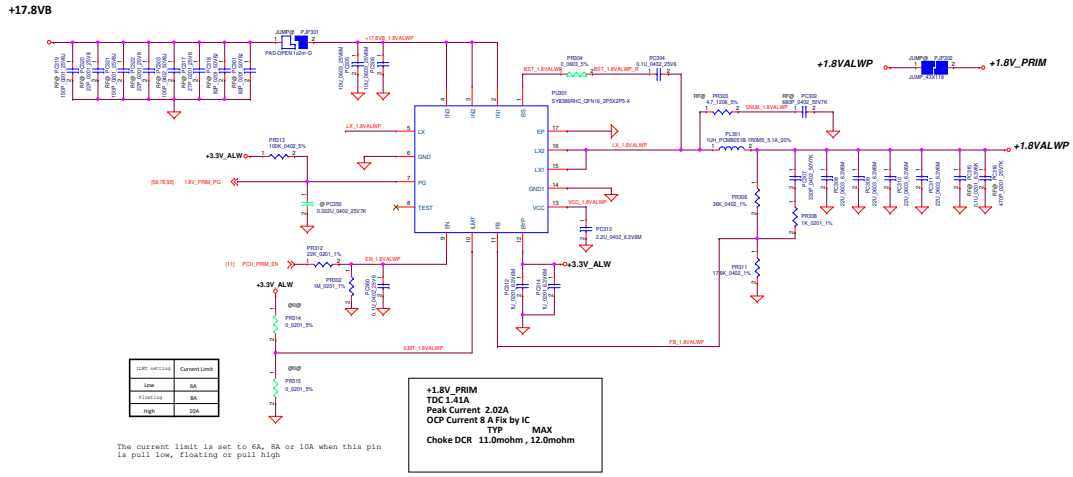

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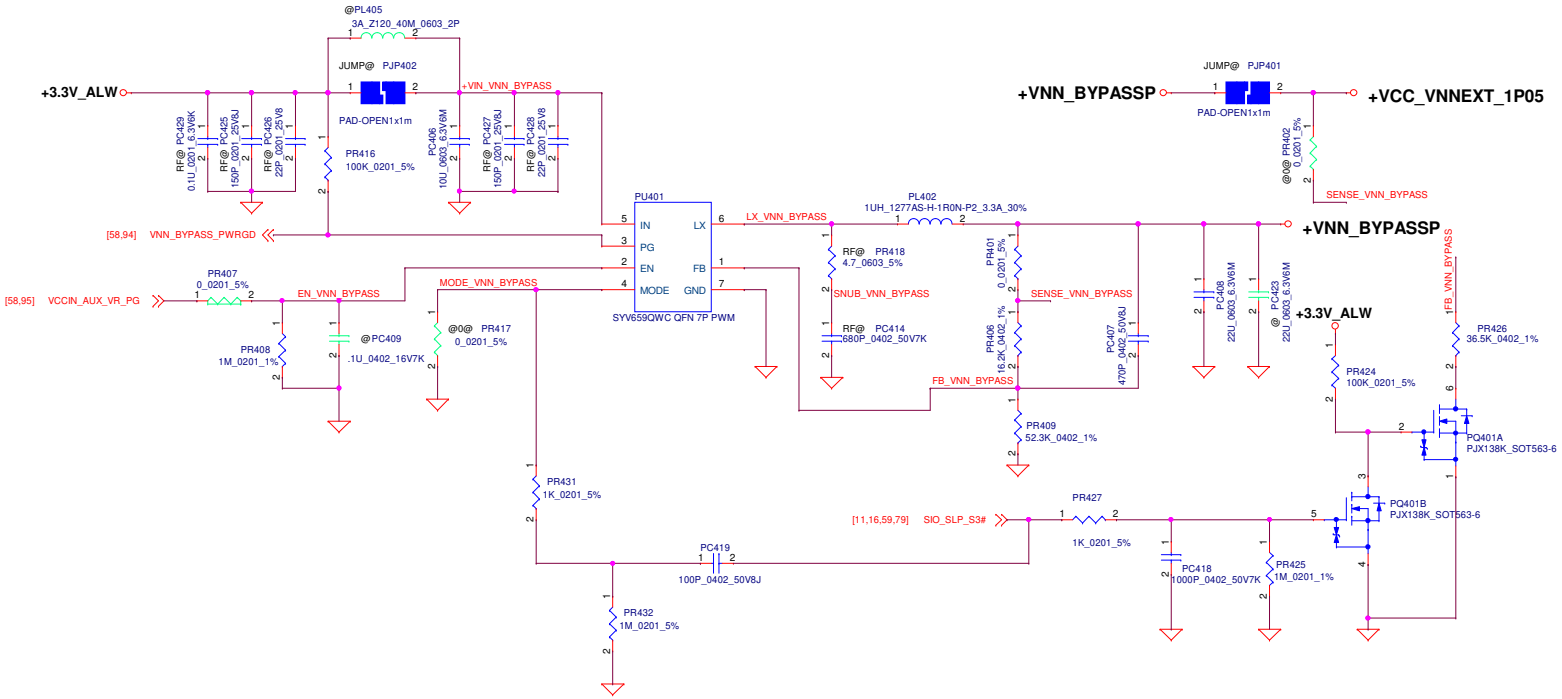

+VNN_BYPASS
TDC 0.105A
Peak Current 0.2 A
OCP Current 3 A

+VNN_BYPASS VR Voltage Configurations
Follow Intel TGL PDG Rev0.9

SLP_S3# State	Output Voltage
Low	1.05
High	0.78

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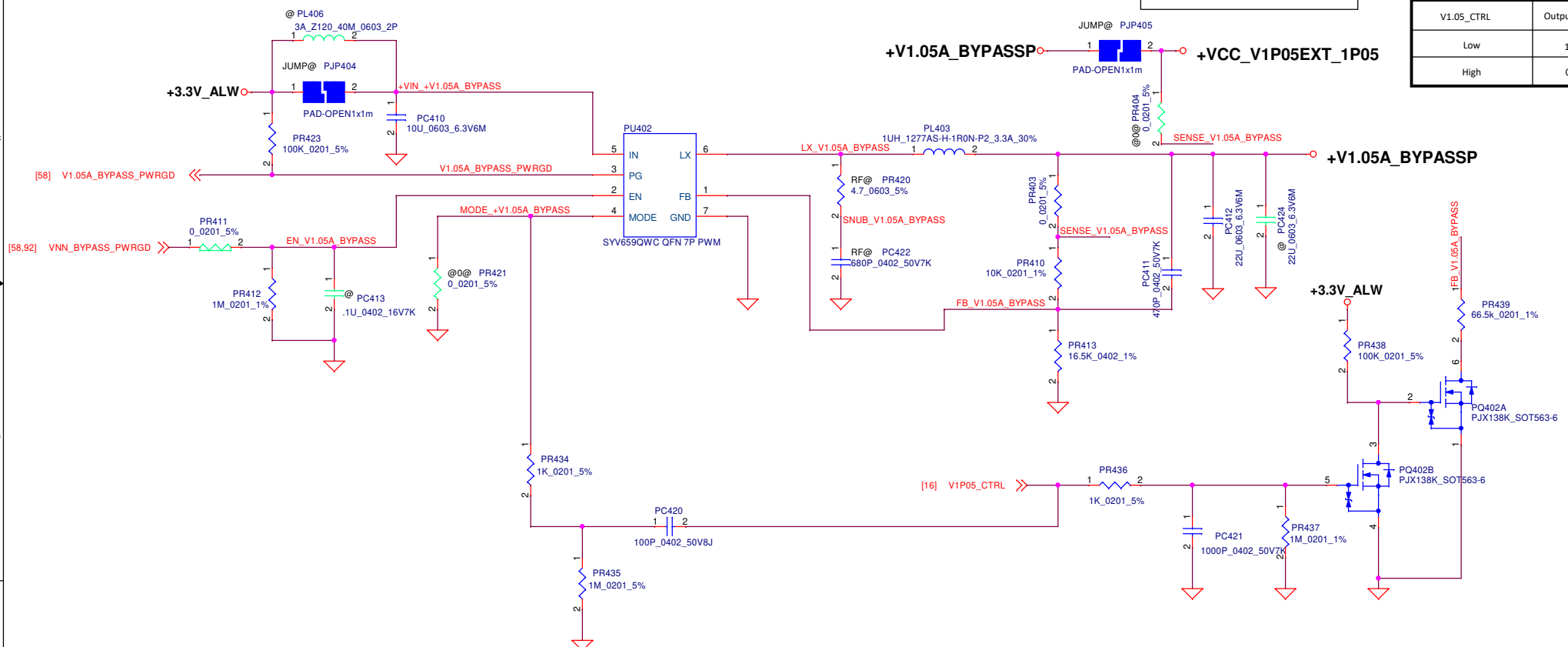

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+VCCIN_AUX
Peak Current 27A (ICCmax)
TDC :14A
DC Load line : NA
AC Load line : NA
Current limit :32A(min) by IC pin.14 setting
Fsw=700kHz

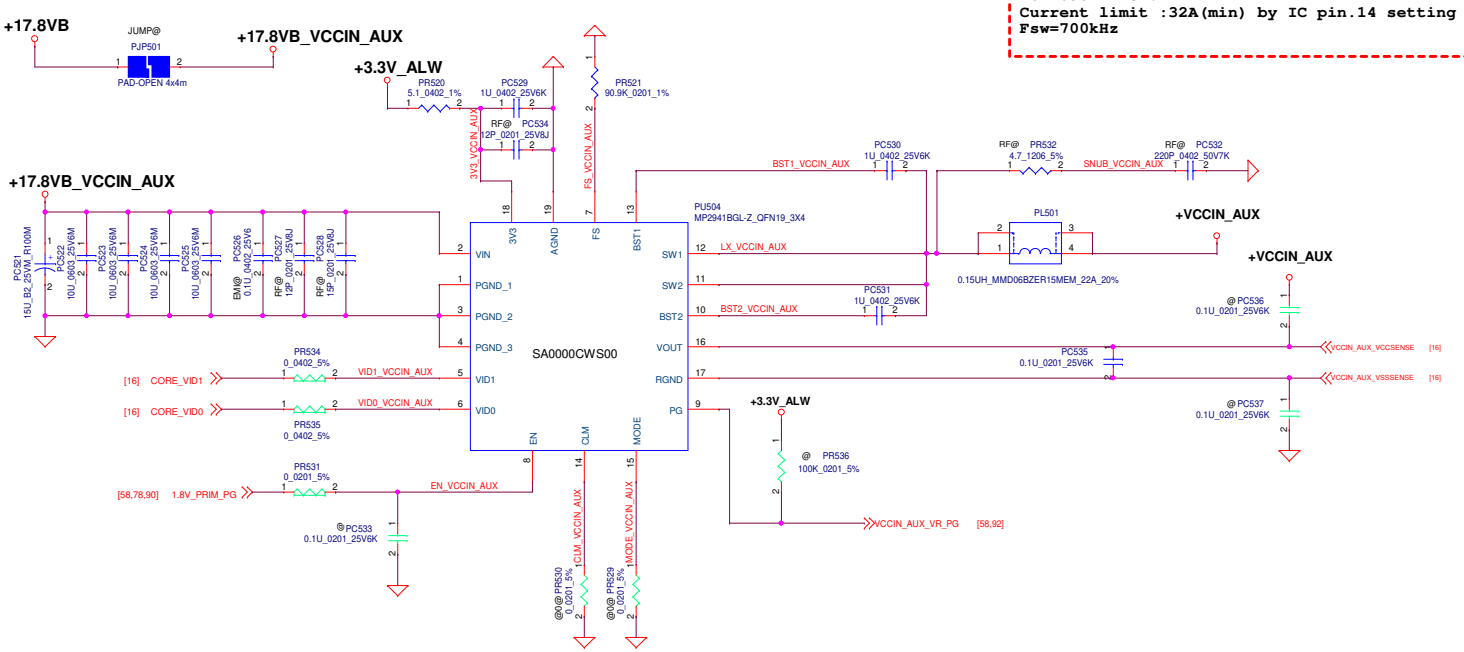

Table---1:VID control Bit logics

VID1	VID0	VOUT(V)
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

Table---2:CLM Select

State	CLM	Resistor to GND
M1	7A	0
M2	10A	90k
M3	13A	150k
M4	16A	>230k or float

Table---3:MODE Select

State	Interleaving	VID Down option	Resistor to GND
M1	N	Slew down	0
M2	Y	Slew down	90k
M3	Y	Decay	150k
M4	N	Decay	>230k or float

Table---4:FS Select

State	Fs(kHz)	Resistor to GND
M1	500	0
M2	700	90k
M3	1000	150k
M4	1200	>230k or float

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Title: +VCCIN_AUX

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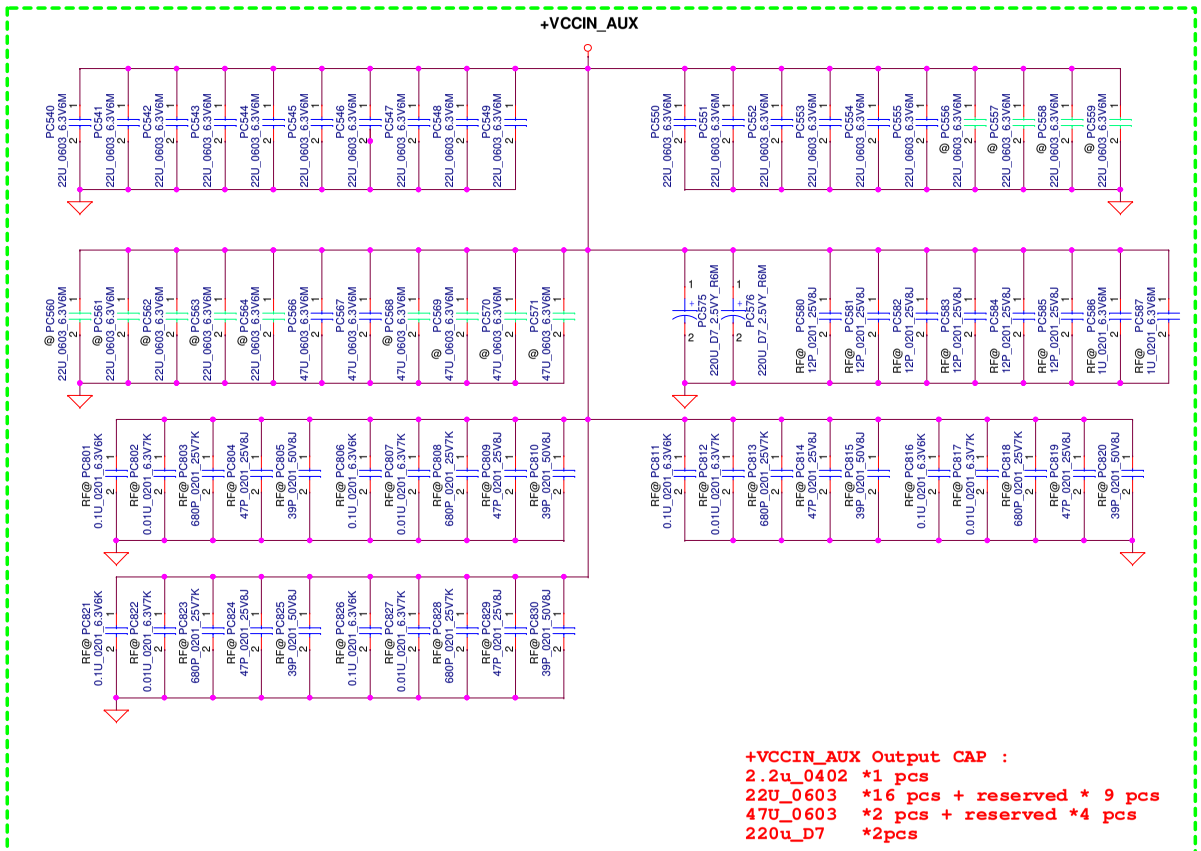

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Title: +VCCIN_AUX Decoupling CAP

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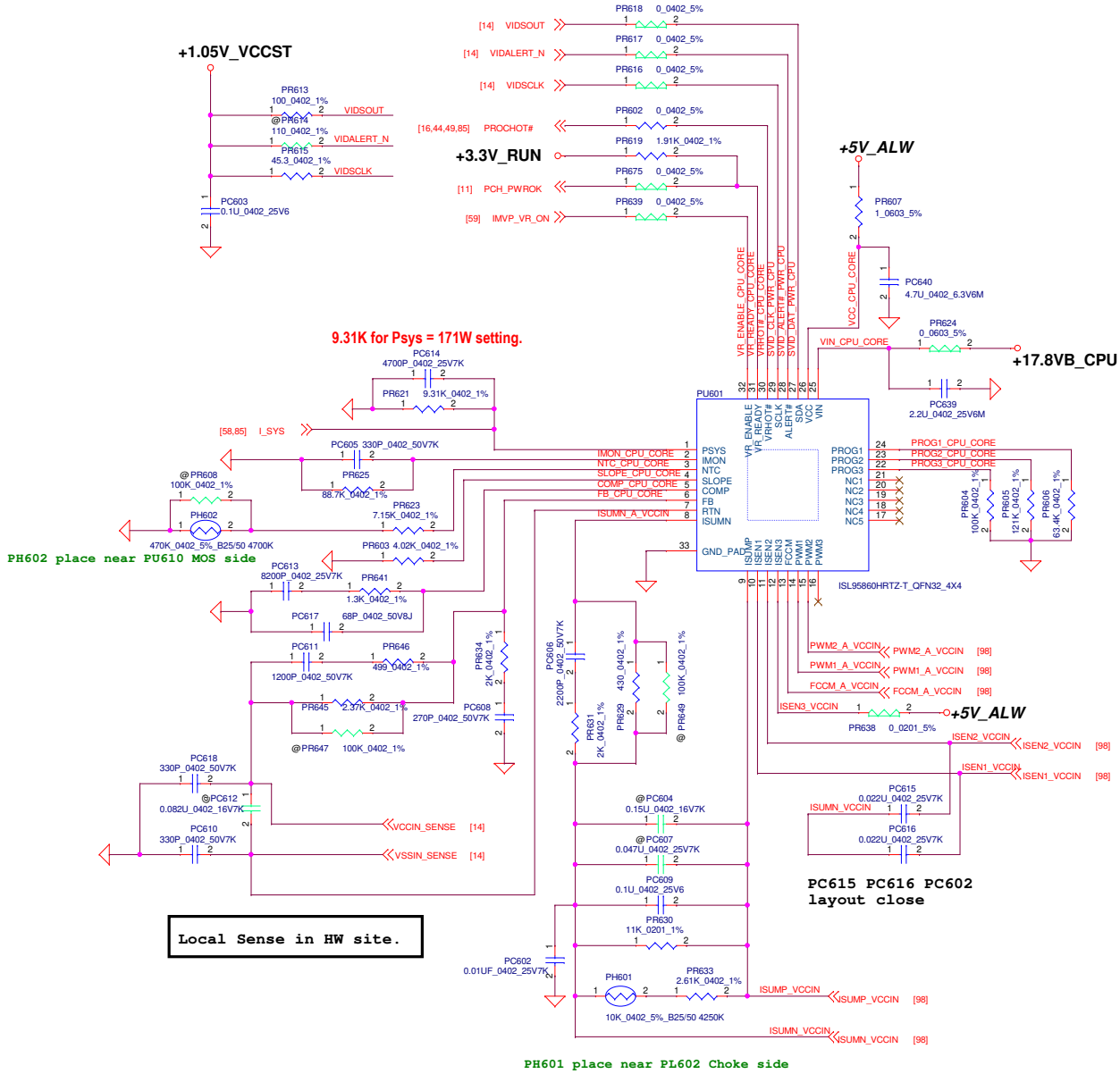

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Title: CPU_CORE

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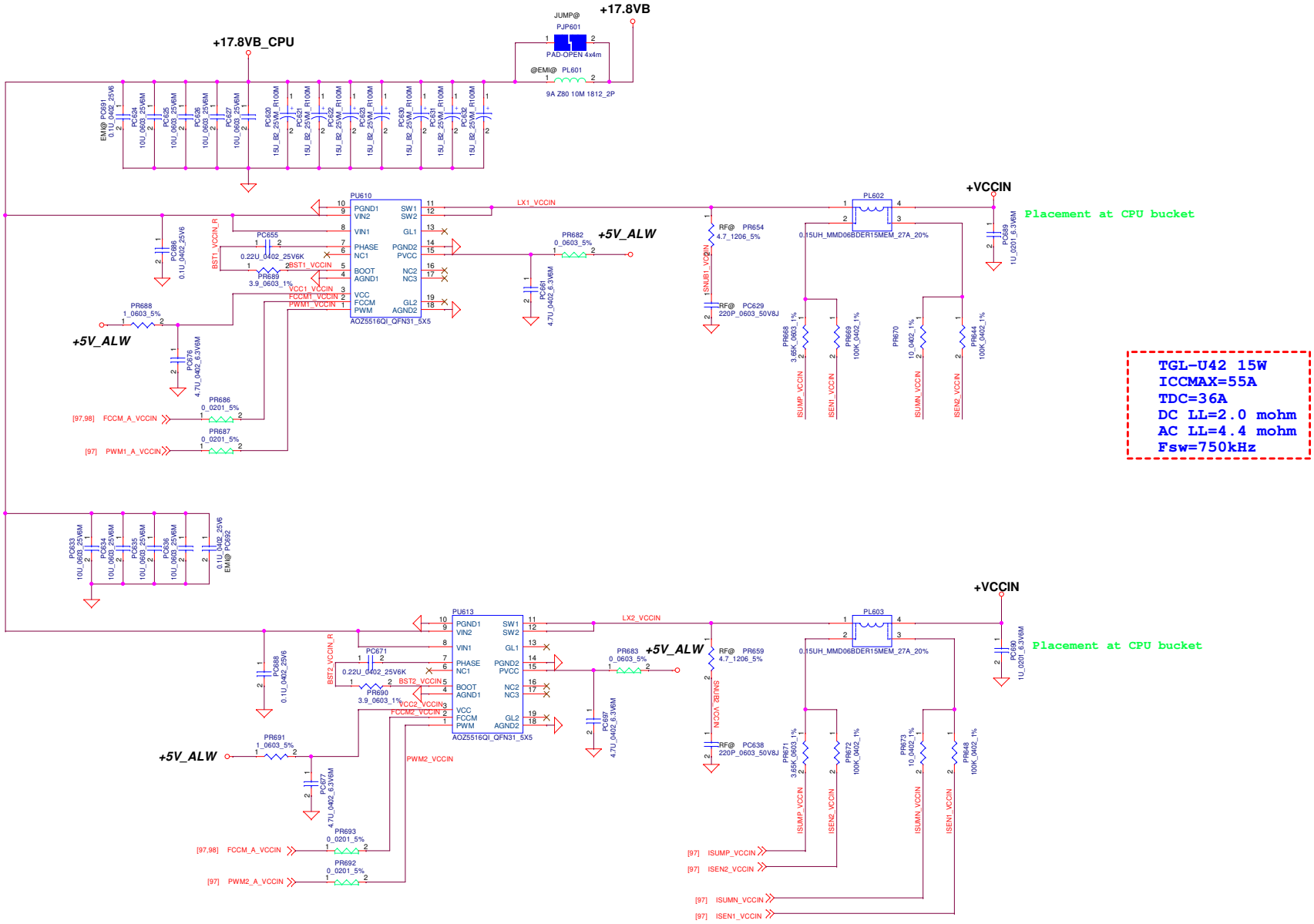
+17.8VB
+17.8VB_CPU
JUMP@
PJP601
PAD-OPEN 4x4m
@EMI@ PL601
9A Z80 10M 1812_2P
PU610
AOZ5516QI_QFN31_5X5
LX1_VCCIN
+5V_ALV
+VCCIN
PL602
0.15UH_MMD06BDER15MEM_27A_20%
Placement at CPU bucket
TGL-U42 15W
ICCMAX=55A
TDC=36A
DC LL=2.0 mohm
AC LL=4.4 mohm
Fsw=750kHz
PU613
LX2_VCCIN
PL603
PWM2_VCCIN
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+VCCIN_SW
LA-K371P
Wednesday, October 28, 2020

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+VCCIN Output CAP :
22U_0603 *14 pcs + reserved *6pcs
220u_D7 *2pcs + reserved *2pcs

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Title: CPU Decoupling CAP		
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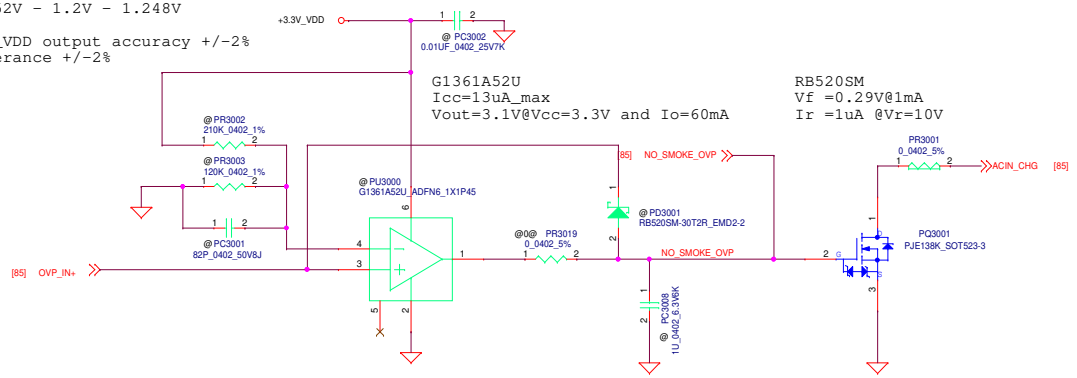
Vf = 1.152V - 1.2V - 1.248V

1. +3.3V_VDD output accuracy +/-2%
2. R tolerance +/-2%



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Item	Page#	Date	Issue Description	Solution Description	Rev.
1	P083 P092 P094	2020/5/12	Net name align with Southpeak	1. +VNN_BYPASS net name change to +VCC_VNNEXT_1P05 2. +VCC_V1P05EXT_1P05V net name change to +VCC_V1P05EXT_1P05 3. B2B name change PQ9 -> S3` PQ10 -> S4 4. V1.05A_CTRL net name change to V1P05_CTRL	X01
2	P083	2020/5/12	B2B solution change to Gen11 solution	1. Add PQ15A, PR94, PR95, PR96, PQ7A, PR91, PR92, PR93 2. PC3, PC16 change to stuff	X01
3	P097	2020/5/19	Vendor request	PR624 change size from 0_0402_5% to 0_0603_5%	X01
4	P096 P101	2020/5/25	RF request	Add 5 sets of MLCC for VCCIN_AUX by RF request, location PC801 ~ PC825 Add 7 sets of MLCC for VCCIN by RF request, location PC851 ~ PC885 * Each set include (0.1U_0201_6.3V, 0.01U_0201_6.3V, 680P_0201_25V, 47P_0201_25V, 39P_0201_50V)	X01
5	P095 P098	2020/5/27	RF request	1. PR532, PC532, PR659, PC638, PR654, PC629 change BS from @EMI@ to RF@ 2. PC532, PC638, PC629 change from 680P_0402_50V to 220P_0402_50V	X01
6	P082	2020/5/28	Reserve for EC study	1. Add PR98 same as PR99 2. PBAT_PRES# net name same as SP	X01
7	P090 P092 P096	2020/5/28	RF request	Add 1 sets of MLCC for VCCIN_AUX by RF request, location PC826 ~ PC830 * Each set include (0.1U_0201_6.3V, 0.01U_0201_6.3V, 680P_0201_25V, 47P_0201_25V, 39P_0201_50V) Add PC319, PC320 12P_0201_25V at PJP301 Add PC425, PC426, PC427, PC428 12P_0201_25V at PJP402	X01
8	P082	2020/5/29	1 key power on solution optimize	Add PQ4004, PR4011, PR4010 for one time power on(LID on but should not power on)	X01
9	P097	2020/5/29	Vender request VRTT tune value	PC607 change to un-stuff PC609 change from 0.033U_0402_25V to 0.1U_0402_25V PR629 change from 649_0402_1% to 430_0402_1%	X01
10	P090 P092	2020/6/1	RF request	PC319, PC425, PC427 change from 12P_0201_25V to 150P_0201_25V PC320, PC426, PC428 change from 12P_0201_25V to 22P_0201_25V	X01
11	P090	2020/6/2	RF request	Add PC321 150P_0201_25V at PJP301 Add PC322 22P_0201_25V at PJP301	X01
12	P082	2020/6/2	New one-shot circuit turn value	PR4040 change from 4.99M_0402_1% to 1M_0402_1% PR4030 change from 1M_0402_1% to 1k_0402_1% PR4034 change from 4.99M_0402_1% to 3M_0402_1% PC4009 change from 0.1U_0402_25 to 0.47U_0402_25V PC4009 change from 0.47U_0402_25V to 1U_0402_6.3V PC4002 change from 1U_0402_25V to 1U_0402_6.3V PR4034 change from 3M_0402_1% to 2M_0402_1%	X01

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EC Chip

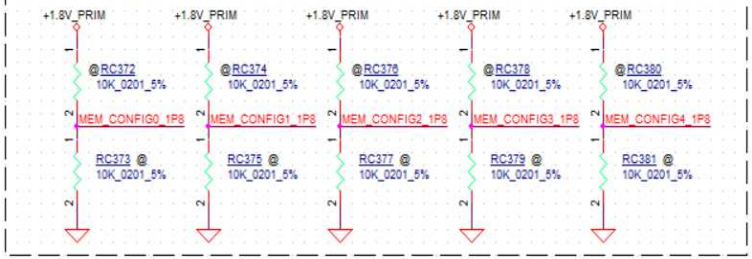
5107ES@ UE1 — MEC5107KD4LJTR_WFBGA176P-NH — SA0000CQ730

5107NES@ UE1 — MEC5107KD4LJTR_WFBGA176P-NH — SA0000CQ740

TPM Chip

750@ UZ12 — NPCT750JADYX — SA0000AQ2C0

DRAM Option Detail at Page 122



X76	DRAM Option	DRAM Config Option (Resistor pop location) MEM_CONFIG0	MEM_CONFIG1	MEM_CONFIG2	MEM_CONFIG3	MEM_CONFIG4
	Samsung 4GB/4266(Channel A only)	UD1 S4G@ SA0000D970L; UD2 S4G@ SA0000D970L	RC373 S4G@ SD043100280	RC374 S4G@ SD043100280	RC376 S4G@ SD043100280	RC379 S4G@ SD043100280	RC380 S4G@ SD043100280
	Samsung 8GB/4266	UD1 S8G@ SA0000D970L; UD2 S8G@ SA0000D970L; UD3 S8G@ SA0000D970L; UD4 S8G@ SA0000D970L	RC373 S8G@ SD043100280	RC374 S8G@ SD043100280	RC376 S8G@ SD043100280	RC379 S8G@ SD043100280	RC381 S8G@ SD043100280
	Samsung 16GB/4266	UD1 S16G@ SA0000D980L; UD2 S16G@ SA0000D980L; UD3 S16G@ SA0000D980L; UD4 S16G@ SA0000D980L	RC372 S16G@ SD043100280	RC375 S16G@ SD043100280	RC377 S16G@ SD043100280	RC378 S16G@ SD043100280	RC381 S16G@ SD043100280
	Samsung 32GB/4266	UD1 S32G@ SA0000D9A0L; UD2 S32G@ SA0000D9A0L; UD3 S32G@ SA0000D9A0L; UD4 S32G@ SA0000D9A0L	RC373 S32G@ SD043100280	RC375 S32G@ SD043100280	RC377 S32G@ SD043100280	RC378 S32G@ SD043100280	RC381 S32G@ SD043100280
	Micron 4GB/4266(Channel A only)	UD1 M4G@ SA0000BX51L; UD2 M4G@ SA0000BX51L	RC373 M4G@ SD043100280	RC375 M4G@ SD043100280	RC377 M4G@ SD043100280	RC379 M4G@ SD043100280	RC380 M4G@ SD043100280
	Micron 8GB/4266	UD1 M8G@ SA0000BX51L; UD2 M8G@ SA0000BX51L; UD3 M8G@ SA0000BX51L; UD4 M8G@ SA0000BX51L	RC373 M8G@ SD043100280	RC375 M8G@ SD043100280	RC377 M8G@ SD043100280	RC379 M8G@ SD043100280	RC381 M8G@ SD043100280
	Micron 16GB/4266	UD1 M16G@ SA0000D4H0L; UD2 M16G@ SA0000D4H0L; UD3 M16G@ SA0000D4H0L; UD4 M16G@ SA0000D4H0L	RC372 M16G@ SD043100280	RC375 M16G@ SD043100280	RC377 M16G@ SD043100280	RC379 M16G@ SD043100280	RC381 M16G@ SD043100280
	Micron 32GB/4266	UD1 M32G@ SA0000D4I0L; UD2 M32G@ SA0000D4I0L; UD3 M32G@ SA0000D4I0L; UD4 M32G@ SA0000D4I0L	RC373 M32G@ SD043100280	RC374 M32G@ SD043100280	RC377 M32G@ SD043100280	RC379 M32G@ SD043100280	RC381 M32G@ SD043100280
	Hynix 4GB/4266(Channel A only)	UD1 H4G@ SA0000DGP0L; UD2 H4G@ SA0000DGP0L	RC372 H4G@ SD043100280	RC374 H4G@ SD043100280	RC377 H4G@ SD043100280	RC379 H4G@ SD043100280	RC380 H4G@ SD043100280
	Hynix 8GB/4266	UD1 H8G@ SA0000DGP0L; UD2 H8G@ SA0000DGP0L; UD3 H8G@ SA0000DGP0L; UD4 H8G@ SA0000DGP0L	RC372 H8G@ SD043100280	RC374 H8G@ SD043100280	RC377 H8G@ SD043100280	RC379 H8G@ SD043100280	RC381 H8G@ SD043100280
	Hynix 16GB/4266	UD1 H16G@ SA0000DGQ0L; UD2 H16G@ SA0000DGQ0L; UD3 H16G@ SA0000DGQ0L; UD4 H16G@ SA0000DGQ0L	RC373 H16G@ SD043100280	RC374 H16G@ SD043100280	RC377 H16G@ SD043100280	RC378 H16G@ SD043100280	RC381 H16G@ SD043100280
	Hynix 32GB/4266	UD1 H32G@ SA0000DGR0L; UD2 H32G@ SA0000DGR0L; UD3 H32G@ SA0000DGR0L; UD4 H32G@ SA0000DGR0L	RC372 H32G@ SD043100280	RC375 H32G@ SD043100280	RC376 H32G@ SD043100280	RC379 H32G@ SD043100280	RC381 H32G@ SD043100280

	LPDDR4x											
supplier	Samsung				Micron				Hynix			
Density	16Gb	16Gb	32Gb	64Gb	16Gb	16Gb	32Gb	64Gb	16Gb	16Gb	32Gb	64Gb
Total MEM size	4GB	8GB	16GB	32GB	4GB	8GB	16GB	32GB	4GB	8GB	16GB	32GB
CPN	SA0000D970L	SA0000D970L	SA0000D980L	SA0000D9A0L	SA0000BX50L	SA0000BX50L	SA0000D4H0L	SA0000D4I0L	SA0000DGP0L	SA0000DGP0L	SA0000DGQ0L	SA0000DGR0L
DPN	15NY1	15NY1	K7HT2	8K7KY	2FG92	2FG92	K7HT2	8K7KY	NCKGR	NCKGR	XG0KR	R45KJ
MPN	K4U6E3S4AA-MGCR	K4U6E3S4AA-MGCR	K4UBE3D4AA-MGCR	K4UCE3Q4AA-MGCR	MT53E512M32D2NP-046WT:E	MT53E512M32D2NP-046WT:E	MT53E1G32D2NP-046WT:A	MT53E2G32D4NQ-046WT:A	H9HCNNNBKMMLXR-NEE	H9HCNNNBKMMLXR-NEE	H9HCNNNCPMMLXR-NEE	H9HCNNNFAMMLXR-NEE
structure	SDP	SDP	DDP	QDP	DDP	DDP	DDP	QDP	DDP	DDP	QDP	ODP
MEM_Config0	0	0	1	0	0	0	1	0	1	1	0	1
MEM_Config1	1	1	0	0	0	0	0	1	1	1	1	0
MEM_Config2	1	1	0	0	0	0	0	0	0	0	0	1
MEM_Config3	0	0	1	1	0	0	0	0	0	0	1	0
MEM_Config4	1	0	0	0	1	0	0	0	1	0	0	0
0 RC372	De-POP	De-POP	POP	De-POP	De-POP	De-POP	POP	De-POP	POP	POP	De-POP	POP
0 RC373	POP	POP	De-POP	POP	POP	POP	De-POP	POP	De-POP	De-POP	POP	De-POP
1 RC374	POP	POP	De-POP	De-POP	De-POP	De-POP	De-POP	POP	POP	POP	POP	De-POP
1 RC375	De-POP	De-POP	POP	POP	POP	POP	POP	De-POP	De-POP	De-POP	De-POP	POP
2 RC376	POP	POP	De-POP	De-POP	De-POP	De-POP	De-POP	De-POP	De-POP	De-POP	De-POP	POP
2 RC377	De-POP	De-POP	POP	POP	POP	POP	POP	POP	POP	POP	POP	De-POP
3 RC378	De-POP	De-POP	POP	POP	De-POP	De-POP	De-POP	De-POP	De-POP	De-POP	POP	De-POP
3 RC379	POP	POP	De-POP	De-POP	POP	POP	POP	POP	POP	POP	De-POP	POP
4 RC380	POP	De-POP	De-POP	De-POP	POP	De-POP	De-POP	De-POP	POP	De-POP	De-POP	De-POP
4 RC381	De-POP	POP	POP	POP	De-POP	POP	POP	POP	De-POP	POP	POP	POP

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Item	Page#	Date	Issue Description	Solution Description	Rev.
1	53	2020/05/18	SIM_DET# net name mistake	Correct DZ13 pin5,6 to SIM_DET	0.2(X01)
2	43	2020/05/18	Add 47uF*1 & Delete 2.2uF*3 for +0.9V_TBT_MB_SVR follow Intel ref design & SP	CT405 change to SE000015500(47uF) from SE00000X880(2.2uF) Delete CT410,CT411	0.2(X01)
3	10,11	2020/05/18	Modify R_0201-X to non-X footprint	RC180,RC205 change footprint	0.2(X01)
4	11,40, 59,78, 79	2020/05/18	Cost down by buyer request	CV49 change to SE00000UC00 from SE00000WV00 CC17,CV65,CV610,CV615,CV616 change to SE00000KD80 from SE00000TF00 CE401,CZ218 change to SE000008880 from SE00000V680 CZ113 change to SE170102K80 from SE00000TG00	0.2(X01)
5	58	2020/05/18	EC SPI_SHARE_BOOT_SELECT change to PD for 5200	RE12 BOM Structure change to 5107@, RE18 BOM Structure change to 5200@	0.2(X01)
6	38,42, 79	2020/05/18	Buyer request	QV2 change to SB00001KM00 from SB00000VD00 YT2 change to SJ10000WZ00 from SJ10000V300 QZ3 change to SB000005F00 from SB000002T00	0.2(X01)
7	10	2020/05/18	Delete redundant component	Delete RC158	0.2(X01)
8	6,40	2020/05/18	Delete redundant component Reserve DDC bypass circuit	Delete CV778,LV602 Reserve RC1,RC2,RV77,RV78,RV81,RV82,QV13	0.2(X01)
9	9,66	2020/05/18	Modify TPM co-lay circuit & add TPM_IDENTIFY for distinguish TPM IC	Add RC399,RC400 connecting to UC1 GPP_E17 (net TPM_IDENTIFY) Delete RZ362; RZ69 change to 100K(SD043100380)	0.2(X01)
10	64	2020/05/18	Modify FPR LED current limit resistor	RZ7,RZ16,RZ17,RZ18 change to 4.99K(SD034499180)	0.2(X01)
11	10	2020/05/18	Delete redundant net	Delete T115,T116	0.2(X01)
12	77	2020/05/18	Screw hole size change by ME request	H10,H12 change to 3P5 from 2P5	0.2(X01)
13	77	2020/05/19	Stand-off & hole size change by ME request	ST5 change to CLIP_C7-D3PM from CLIP_C8 H5 change to H_3P5 from H_4P0 ST1,ST2 change to CLIP_C6P5-D3PM from CLIP_C6P5	0.2(X01)
14	16	2020/05/19	Update PWR circuit0519A	1. +VNN_BYPASS net name change to +VCC_VNNEXT_1P05 2. +VCC_V1P05EXT_1P05V net name change to +VCC_V1P05EXT_1P05 3. V1.05A_CTRL net name change to V1P05_CTRL 4. Power path follow Gen11 solution 5. PU102 footprint modify 6. BOM change	0.2(X01)
15	64	2020/05/19	Modify ESD requirement	DC9 pin3 change to MCD_PW	0.2(X01)
16	53	2020/05/19	Modify RF requirement	LI16,LI17 change to pop, RZ1523~RZ1526 change to unpop	0.2(X01)
17	40	2020/05/19	Modify HDMI EA fail item	LV12 change to pop, RV62,RV63 change to unpop	0.2(X01)
18	59	2020/05/19	Modify Board ID	RE79 change to 130K ohm(SD028130380) from 240K ohm	0.2(X01)
19	42	2020/05/22	Optimize 25MHz Crystal Clk	CT42,CT43 change to 27pF(SE174270J80) from 18pF(SE000004H00)	0.2(X01)
20	53	2020/05/27	Modify RF requirement	RZ1533 change to unpop	0.2(X01)
21	11,58, 64	2020/05/27	Buyer request	QZ7,QZ22,QZ23 change to SB000009Q80 from SB00001CS00 RE94 change to SD000012A80 from SD000012AZ0 YC2 change to SJ10000PW00 from SJ100011U00	0.2(X01)
22	12,38, 56,66, 71	2020/05/27	ESD request to change main source	DA2 change to SCA00004320 from SCA00001A00 DA6,DA7,DZ108 change to SCA00002X00 from SCA00002A00 DZ11 change to SCA00002X00 from SCA00004300 DI5,DV13,DV14,DZ10,DZ21 change to SCA00002X00 from SCA00004700	0.2(X01)

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Item	Page#	Date	Issue Description	Solution Description	Rev.
23	PWR	2020/05/27	Update PWR circuit0527A	Add PC801 ~ PC825, PC851 ~ PC885 by RF request VCCIN_AUX, VCCIN snubber change to stuff by RF request	0.2(X01)
24	56	2020/05/27	EMI request	CA19,CA22,CA23,CA24 change to pop 680pF(SE00000XA80)	0.2(X01)
25	77	2020/05/28	Hole size change by ME request	H6,H7 change to H_3P5 from H_4P0	0.2(X01)
26	6,40	2020/05/28	Change component size to 0201	RV77,RV78,RV81,RV82,RC1,RC2 change to 0201	0.2(X01)
27	58 PWR	2020/05/28	Update PWR circuit0528B	Add PR98 reserve for EC study PBAT_PRES PBAT_PRES# net name change to PBAT_PRES#_GPIO175 Add new net name PBAT_PRES_GPIO101 Add RF request part	0.2(X01)
28	PWR	2020/05/29	Update PWR circuit0529A	1. One-time power on from storage mode circuit modify 2. BOM change	0.2(X01)
29	77	2020/06/01	Update Screw Hole	H15 change to PTH(connect to GND)	0.2(X01)
30	53	2020/06/01	Modify RF requirement	Reserve DT41 for RF request	0.2(X01)
31	PWR	2020/06/01	Update PWR circuit0601A	BOM change(RF)	0.2(X01)
32	PWR	2020/06/02	Update PWR circuit0602A	1. Add PC321、PC322 for RF request 2. BOM change	0.2(X01)
33	13	2020/06/08	Update CNVI checklist	RC265 change to 100K(SD043100380) from 47K	0.2(X01)
34	16	2020/06/08	Update +VCCLDOSTD_OUT_0P85 Cap following PDG	CC66 change to SE00000W100 for 10% tolerance	0.2(X01)
35	44,49	2020/06/08	PD ROM change to unpop for combine to BIOS ROM	UPD3,UPD5(SA000088F00) change to unpop	0.2(X01)
36	122	2020/06/10	Change Nuvoton TPM CPN	UZ12 change to SA0000AQ2C0 from SA0000AQ220	0.2(X01)
37	9,11	2020/06/10	Change BOM to follow SP	RC132 change to 4.7K from 100K RC187 change to 20K from 10K	0.2(X01)
38	64	2020/06/10	Change LED Current limit RES	RZ361,RZ28 change to 300ohm from 1.5Kohm	0.2(X01)
39	66	2020/06/12	Change ACC Sensor LIS2DW12 Pin3 PD RES for under VIL	RZ155 change to 1K(SD043100180) from 10K(SD043100280)	0.2(X01)
1	66	2020/08/11	Correct DZ11 footprint	DZ11 footprint change to CEST523NC5VB_SOT-523-3	0.3(X02)
2	66	2020/08/11	Correct CZ55 BOM Structure	CZ55 BOM Structure change to NA	0.3(X02)
3	59	2020/08/11	Update Board ID	RE79 change to 62K ohm	0.3(X02)
4	9	2020/08/11	Change BIOS ROM to 75% DRIVING part	UC2 change to SA0000DUA00	0.3(X02)
5	59	2020/08/11	Modify for RTC power consumption	RE88 change to 2M ohm from 100k ohm	0.3(X02)
6	44,49, 58	2020/08/11	Correct net name for reasonable	UPD1_SMBINT#_R change to UPD1_SMBINT#_MB UPD1_SMBINT# change to UPD1_SMBINT#_IO	0.3(X02)
7	53	2020/08/11	WWAN_FULL_PWR_EN reserve Rpd to align with SP	Reserve RZ172(100K)	0.3(X02)
8	40, PWR	2020/08/14	HDMI reserve POWERSW pin Update PWR circuit 0814A	Reserve HDMI_1.2V_EN pin to enable +1.2V_RUN	0.3(X02)
9	64	2020/08/17	Adjust LED limit Res	RZ28, RZ361 change to 150 ohm from 300 ohm	0.3(X02)
10	79	2020/08/17	Adjust M_BIST Res for align with SP	RZ1482 change to 330K ohm from 1M ohm	0.3(X02)
11	9	2020/08/17	Modify for DXF request	DC1 Footprint change to SCS00007I00's footprint	0.3(X02)
12	77	2020/08/17	Modify Screw hole for ME request	ST3,ST4,ST5 change to CLIP_C6P5-D3PM; H7 change to H3P8 from H3P5	0.3(X02)
13	16	2020/08/17	Modify VCCSTG reserved control according to PDG	Change RC299.1 net to SIO_SLP_S3# from SIO_SLP_S0#	0.3(X02)
14	64	2020/08/24	Adjust FPR Current Limit Resistor	Change RZ7,RZ16,RZ17,RZ18 to 1.2k from 4.99k ohm	0.3(X02)

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Version Change List (P. I. R. List)

Item	Page#	Date	Issue Description	Solution Description	Rev.
15	38,43,53,56,58,78	2020/08/24	Modify for RF request	Reserve CE75(0.1uF)+CE76(680pF) for +3.3V_ALW Reserve CZ399(0.1uF)+CZ401(0.1uF)+CZ400(680pF)+CZ402(680pF) for +3.3V_WWAN Reserve snubber RT666(4.7ohm)+CT457(680pF) for +3.3V_TBT_MB_L Reserve CZ403(1uF) for +3.3V_RUN_UZ3 Reserve CZ404(1uF) for +5V_RUN_UZ47 CA68 change to 15pF from 68pF; CV752 change to 0.1uF from 100pF	0.3(X02)
16	PWR	2020/08/24	Update PWR circuit0824A	Reserve PC586, PC587, PC1037, PC1038, PC1039, PC4040, PC429, PC142, PC143 for RF request RF BOM change	0.3(X02)
17	PWR	2020/08/25	Update PWR circuit0825A	re-link PL100, PL101 CIS symbol Reserve PC527, PC528, PC534 for RF request RF BOM change	0.3(X02)
18	PWR	2020/08/26	Update PWR circuit0826A	PL100, PL101 footprint modify	0.3(X02)
19	16	2020/08/26	Modify PROCHOT# circuit for VRLAERT# voltage issue	RC297 change to 10K; RC395 change to 100K	0.3(X02)
20	10,58	2020/08/27	Eanble TOP SWAP feature	Delete RE561 RC160 change to Pop RC170 change to pop 4.7k	0.3(X02)
21	79	2020/08/27	Adjust M_BIST Res for align with SP	RZ1482 change back to 1M ohm from 330K ohm	0.3(X02)
22	PWR	2020/08/28	Update PWR circuit0828A	Add PC535 for vendor request	0.3(X02)
23	PWR	2020/08/29	Update PWR circuit0829B	1. Remove PR525, PR526 2. PC535 BS change to @RF@	0.3(X02)
24	52	2020/09/01	WLAN change to R3 Part	WL1 change to PK29S00AY7L from PK29S00AY6L	0.3(X02)
25	79	2020/09/01	Cost down M-BIST circuit	QZ3,RZ25 change to un-pop; QZ27 change to pop	0.3(X02)
26	15	2020/09/02	Reserve 0201 MLCC on +1.1V_MEM by Intel request	Reserve CC106~CC109 on +1.1V_MEM	0.3(X02)
27	PWR	2020/09/02	Update PWR circuit0902A	Add PC536, PC537	0.3(X02)
28	PWR	2020/09/02	Update PWR circuit0902B	1. PR208, PR210, PR513, PR531 change from 0 ohm short pad to 0 ohm 2. BOM change	0.3(X02)
29	PWR	2020/09/03	Update PWR circuit0903A	Add PR4050 and more circuit for one shot support circuit	0.3(X02)
30	6	2020/09/03	Modified BOM structure for TBT_LSX_RX by Intel recommend	RC15,RC16 change to un-pop	0.3(X02)
31	38,66	2020/09/07	Modify BOM for Sourcer request	Change QV8,QV22,QV23,QZ1,QZ18 to SB000017J00 from SB00000SS00	0.3(X02)
32	PWR	2020/09/09	Update PWR circuit0907B	BOM Change	0.3(X02)
1	59	2020/10/19	Update board ID version to A00	Change value of locaiotn RE79 to 4.3K_0402_1% from 62K_0402_1%	1.0(A00)
2	58	2020/10/19	Change BOM structure for un-uesd GPIO	RE552 change to unpop from pop	1.0(A00)
3	58,63	2020/10/19	Add AND-Gate for PCH_DPWROK to modify sequence according to PDG2.1	1. Add UZ19,CZ132 2. RE536 change to un-pop	1.0(A00)
4	PWR	2020/10/19	Update PWR circuit1013A	1. PR14,PR84,PR85,PR208,PR210,PR407,PR411,PR513,PR531,PR719,PR747,PR753,PR754,PR4009,PR4010,PR4026,PR4048 change from 0 ohm short pad to 0 ohm 2. BOM change	1.0(A00)
5	44,49	2020/10/20	Reseved resistor for leakage issue according to vendor's suggestion	1. Add RT667(100k) for UPD2 pin32 2. Add RT668(100k) for UPD4 pin32	1.0(A00)
6	ALL	2020/10/20	Change 0 ohm to short pad Change 0.01 ohm to short pad	Change to short pad==>RC282,RC283,RC284,RC298,RC309,RC312,RC336,RT1,RT180,RT181,RT578,RT618 Footprint change to -NPM==>LV13,LV14,LV15,LV16,LV17,RZ1523,RZ1524,RZ1525,RZ1526,RV101,CI32,RN130,LV3,LV6,LV9,RV62,RV63	1.0(A00)
7	79	2020/10/23	Change SWME to unpop for MP	1. SWME1,RC222 change to unpop 2. RC221 change to short pad	1.0(A00)
8	66	2020/10/23	Modify for Lid close issue	1. DZ105 change direction 2. RC388 change to unpop	1.0(A00)
9	64	2020/10/23	Modify for align with SP	RZ3, RZ1531 change to 2M from 1M	1.0(A00)

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